WELCOME TO ICECS 2012

GENERAL CHAIRS'S MESSAGE

On behalf of the Organizing Committee of ICECS 2012, and of my co-chairs Dr. Manuel Delgado-Restituto and Prof. Magdy Bayoumi, it is my pleasure to welcome you to the 19th International Conference on Electronics, Circuits, and Systems, to Seville and to Spain. ICECS 2012, sponsored by the Institute of Electrical and Electronics Engineers, is the flagship conference of the IEEE Circuits and Systems Society in Region 8. The ICECS series of conferences have evolved during nearly two decades to become a major networking event for those working on CASS topics, from analog and RF circuits to VLSI signal processing, including biomedical, emerging technologies, CAD, nonlinear and neural networks, etc. As a delegate at ICECS 2012 you will have the opportunity to learn of the latest advances in these fields, and to meet those who have dared, pioneered, and succeeded.

The conference is to be held at the Barceló Hotel Renacimiento, on the Isla de la Cartuja, an island located between two branches of the Guadalquivir river which today is home to the Cartuja 93 technology business park. Seville's downtown (El Centro) is very close by and, from there, visitors will find Seville's major monuments and shops just a few short steps away.

This year, a total of 380 submissions from 51 different countries were received including 222 papers from Europe, 61 from Asia-Pacific, 28 from North America, 26 from Latin America and 43 from the Middle East and Africa. This is proof of the truly international nature of this event.

The Technical Program has been selected with the inestimable, volunteer support of 31 Track Chairs coordinated by Prof. de la Rosa and Prof. Setti; many thanks to all them. They have been backed by more than 300 anonymous reviewers whose contribution has been instrumental for the conference. Three plenary presentations by guest speakers complete the program by focusing on highly relevant topics selected by an ad-hoc committee. I would like to thank these guest speakers for their availability.

As a novelty this year, seven Tutorials covering a variety of topics will be made available for free to all attendees. The service to society rendered by these lecturers in making their expertise openly available deserves my highest recognition.

I would also like to thank the Steering Committee of ICECS for giving us the opportunity to host this event. The conference has been organized by members of the Institute of Microelectronics

WELCOME TO ICECS 2012

GENERAL CHAIRS'S MESSAGE

of Seville (IMSE-CNM), the Spanish Council of Research (CSIC) and the University of Seville. I would like to thank the authorities of these institutions for allowing all us to devote part of our time to the organization of this conference.

Many thanks as well to my Conference Co-Chairs, Dr. Manuel Delgado-Restituto and Prof. Magdy Bayoumi for their inestimable advice and support. The three of us have been extremely fortunate to count on an outstanding team of volunteers of the Organizing Committee, who have all worked very hard. We are hugely indebted to all these volunteers. Our warm thanks to all of them for their dedication, enthusiasm and professionalism.

Last but not least, we would like also to express our greatest appreciation to all the authors who submitted papers to the conference and to all delegates, tutorial lecturers and plenary speakers who have travelled to Seville to interact and share their thoughts during the Conference. They will play a leading role at the event.

Enjoy ICECS 2012 and your visit to Seville. I hope to see you all back here more often!

Welcome / Bienvenidos !!

Ángel Rodríguez-Vázquez
University of Seville
General Chair - ICECS 2012

ABOUT IMSE/US

The “Instituto de Microelectrónica de Sevilla” (IMSE) is a R&D center specialized on design and test of analog, mixed-signal, and sensory-processing integrated circuits as well as on their use in any application context, specially in RF, microsystems, data conversion, ...

IMSE, together with the Microelectronics Institutes in Barcelona (IMB) and Madrid (IMM), form the Spanish National Microelectronics Center (CNM) operated under the umbrella of “Consejo Superior de Investigaciones Científicas” (CSIC).

The personnel from IMSE has been carrying out research, teaching, and technology transfer for more than 20 years. In particular, teaching is done as regular courses offered by the University of Seville and as courses and seminars given elsewhere on demand. The PhD thesis and the research projects within IMSE are mainly focusing on the implementation of innovative concepts in silicon, paying special attention to their experimental verification.

Starting on 2009, IMSE is providing external services based on a tester Agilent 93000, giving training, technical support, and test-board design for implementing and debugging test procedures both in analog and digital.

In addition, IMSE offers an academic master: *Master in Microelectronics Design and Applications of Micro/Nanometric Systems*. It is oriented to provide professionals with a scientific, technological, and sociol-economic education in Micro-Nano electronics.

On the other hand, the “Universidad de Sevilla” (US) is a top-ranked European university. Founded under the name of Colegio Santa María de Jesús in 1505, the University of Seville, with a student body of over 55,000, is one of the most important higher education institutions in the country.

The Faculties, Technical High Schools, Polytechnics and University Schools are the centers in charge of organizing the teaching as well as the academic, administrative, and managerial processes leading to obtaining a degree.

Public service of higher education is assigned to this university and carried out through the study, teaching and research as well as through the generation, development and diffusion of knowledge at society and citizenship’s service, offering as well, scientific and technical support for the cultural, social, economic and territorial development and the concern for training professionals.

CONTENTS

OVERVIEW OF ICECS 2012

The IEEE International Conference on Electronics, Circuits, and Systems (ICECS) is the flagship conference of the IEEE Circuits and Systems (CAS) Society in Region 8 of IEEE (Europe, Middle East, and Africa). Papers from all over the world are presented on design methodologies, techniques and experimental results in emerging electronics, circuits, and systems.

Technical Sessions

IEEE ICECS 2012 sessions will cover all aspects of the fields of electronics, circuits, and systems, including analog and digital electronics, solid-state circuits, green and power electronics, biomedical and life-science circuits and systems. Topics include, but are not limited to:

- Analog & Mixed Signal Circuits and Signal Processing
- Bioengineering Circuits and Systems
- Circuits and Systems for Communications
- Digital Circuits and Signal Processing
- Emerging Technologies (Nano, MEMS)
- Low-Power and Harvesting Techniques
- Multimedia Systems and Signal Processing
- Neural Network Circuits and Systems
- Nonlinear Circuits and Systems
- Photonic and Optoelectronic Circuits
- Sensing and Sensor Networks
- Test and Reliability
- VLSI Systems, Applications, and Computer Aided Network Design

Plenary Lectures

In addition to contributed papers, the event will include plenary lectures and tutorials. Three exciting plenary lectures presented by world-wide recognized experts has been organized to cover hot topics in the circuits and systems field.

Tutorials

In an attempt to increase the number of attendees and create a fruitful pre-conference atmosphere, the Organization has made a great effort to offer these short courses for free. The seven tutorials are scheduled.

Social Program

An attractive social program will accompany the event, featuring a welcome reception, a gala dinner, a farewell reception, and excursions.

CONFERENCE SCHEDULE

Sunday, December 9th, 2012

09:00	Morning Tutorials
11:00	Break
11:30	Morning Tutorials (cont.)
15:00	Afternoon Tutorials
17:00	Break
17:30	Afternoon Tutorials (cont.)

Monday, December 10th, 2012

08:15	Conference Opening
08:30	Plenary Lecture
09:30	Lecture Sessions
11:10	Coffee Break
11:30	Lecture Sessions
13:10	Lunch
14:40	Lecture Sessions
16:20	Coffee Break
16:40	Poster Briefing Session 1
17:10	Lecture Sessions
19:30	Welcome Reception

Tuesday, December 11th, 2012

08:30	Plenary Lecture
09:30	Lecture Sessions
11:10	Coffee Break
11:30	Lecture Sessions
13:10	Lunch
14:40	Lecture Sessions
16:20	Coffee Break
16:40	Poster Briefing Session 2
17:10	PhD Competition and Poster Exhibition
19:30	Gala Dinner

Wednesday, December 12th, 2012

08:30	Plenary Lecture
09:30	Lecture Sessions
11:10	Coffee Break
11:30	Lecture Sessions
13:10	Lunch
14:40	Lecture Sessions
16:20	Coffee Break
16:40	Lecture Session
18:20	Closing Ceremony

MEETING ROOMS FLOORPLAN

MEETING ROOMS FLOORPLAN

PROGRAM AT A GLANCE

SUNDAY, DECEMBER 9th, 2012				
Time	**Room Andalucía 5**	**Room Andalucía 6**	**Room Andalucía 7**	**Room Andalucía 8**
09:00-11:00	**TUTORIAL 1** **Advances in Time-Encoded Analog Signal Processing and Data Conversion** L. Hernández, S. Paton, E. Prefasi (Carlos III Univ.) - P. Rombouts (Gent Univ.)	**TUTORIAL 2** **Siliconized Photonics-Electronics as an Emerging Technology** Henry H. Radamson, Lars Thylén (KTH)	**TUTORIAL 3** **RF CMOS Wireless Receivers for 402MHz Medical Implantable Communication Systems** S. Mohamed, Y. Manoli (Albert-Ludwig-University Freiburg)	
11:00-11:30	BREAK			
11:30-13:00	**TUTORIAL 1 (cont.)**	**TUTORIAL 2 (cont.)**	**TUTORIAL 3 (cont.)**	
15:00-17:00	**TUTORIAL 4** **Digital Delta-Sigma Modulators for DAC and Fractional-N Frequency Synthesis Applications** Michael Peter Kennedy (Univ. College Cork)	**TUTORIAL 5** **Using Logical Effort for Designing Carbon Nanotube FET (CNFET)-based Digital Circuits** Malgorzata Chrzanowska-Jeske (Portland State Univ.)	**TUTORIAL 6** **Memristor Technology in Neuromorphic Circuits** Fernando Corinto (Politecnico di Torino)	**TUTORIAL 7** **Low Power Design Methodology and Techniques – Industrial Perspective** Kaijian Shi (Cadence Design Systems, USA)
17:00-17:30	BREAK			
17:30-19:00	**TUTORIAL 4 (cont.)**	**TUTORIAL 5 (cont.)**	**TUTORIAL 6 (cont.)**	**TUTORIAL 7 (cont.)**

MONDAY, DECEMBER 10th, 2012					
Time	**Room Sevilla I**	**Room Andalucía 8**	**Room Andalucía 7**	**Room Andalucía 6**	**Room Andalucía 5**
08:15-08:30	ROOM Sevilla I - CONFERENCE OPENING (Prof. Ángel Rodríguez-Vázquez)				
08:30-09:20	ROOM Sevilla I - PLENARY LECTURE: Ultra-Low Power Circuit Techniques for Implanted/Medical Applications SPEAKER: Prof. Yusuf Leblebici (EPFL)				
09:30-11:10	**A1L-A** Analog Circuits and Techniques I	**A1L-B** Bioengineering Circuits and Systems I	**A1L-C** Digital Signal Processing	**A1L-D** RF Building Blocks	**A1L-E (SPECIAL SESSION)** Computationally Intensive Applications on FPGAs
11:10-11:30	COFFEE BREAK				
11:30-13:10	**A2L-A** Analog Circuits and Techniques II	**A2L-B** Sensing and Sensor Networks	**A2L-C** DSP Algorithm and Implementation	**A2L-D** RF and mmWave Circuits	
13:10-14:40	LUNCH				
14:40-16:20	**A3L-A** Analog Circuits and Techniques III	**A3L-B** Sensors and Photonics	**A3L-C** Digital Circuits on FPGAs	**A3L-D** Wireless and Wireline Communications	
16:20-16:40	COFFEE BREAK				
16:40-17:10	**B4P-G** Poster Briefing Session 1				
17:10-18:50	**A4L-A** Analog Filters	**A4L-B** Mixed-Signal Test and Verification	**A4L-C** VLSI Digital Implementations	**A4L-D** Algorithms for Communications	**A4L-E (SPECIAL SESSION)** Advances in Embedded Vision Hardware
19:30	WELCOME RECEPTION				

PROGRAM AT A GLANCE

TUESDAY, DECEMBER 11th, 2012				
Time	**Room Sevilla I**	**Room Andalucía 8**	**Room Andalucía 7**	**Room Andalucía 6**
08:30-09:20	ROOM Sevilla I - PLENARY LECTURE: From Data to Insight SPEAKER: Dr. Ellen J. Yoffa (IBM)			
09:30-11:10	**B1L-A** Data Converters	**B1L-B** Bioengineering Circuits and Systems II	**B1L-C (SPECIAL SESSION)** Digital Circuits for Embedded Control and Security	**B1L-D** Digital Circuits for Channel Coding
11:10-11:30	COFFEE BREAK			
11:30-13:10	**B2L-A** Oversampling Data Converters	**B2L-B** Analysis and Design for Low-Power Circuits	**B2L-C** Circuit Level CAD	**B2L-D** Nonlinear Circuits and Systems I
13:10-14:40	LUNCH			
14:40-16:20	**B3L-A** Nyquist Rate Data Converters	**B3L-B** Circuit Techniques for Energy Harvesting Applications	**B3L-C** Methodologies for Systems-on-Chip	**B3L-D** Multimedia Systems and Signal Processing I
16:20-16:40	COFFEE BREAK			
16:40-17:10	**B4P-H** Poster Briefing Session 2			
17:10-19:10	**BA4L-A** PhD Competition	Poster area - POSTER EXHIBITION		
19:30	GALA DINNER			

WEDNESDAY, DECEMBER 12th, 2012				
Time	**Room Sevilla I**	**Room Andalucía 8**	**Room Andalucía 7**	**Room Andalucía 6**
08:30-09:20	ROOM Sevilla I - PLENARY LECTURE: Compressed Sensing Analog-to-Digital Conversion SPEAKER: Prof. Michael Flynn (University of Michigan)			
09:30-11:10	**C1L-A** RF Circuits and Techniques I	**C1L-B** Emerging Technologies I	**C1L-C** Digital Test, Fault Tolerance and Reliability	**C1L-D** Multimedia Systems and Signal Processing II
11:10-11:30	COFFEE BREAK			
11:30-13:10	**C2L-A** RF Circuits and Techniques II	**C2L-B** Emerging Technologies II	**C2L-C** Variability-Aware Design and Noise Mitigation	**C2L-D** Nonlinear Circuits and Systems II
13:10-14:40	LUNCH			
14:40-16:20	**C3L-A** Power Management Circuits	**C3L-B** Neural Networks and Nonlinear Circuits	**C3L-C** Energy Efficient High-Level Design and Modeling Techniques	**C3L-D** Communication Algorithms and Building Blocks
16:20-16:40	COFFEE BREAK			
16:40-18:20	**C4L-A** Sensors and Imagers	**C4L-B (SPECIAL SESSION)** Advances in Nanoscale Devices and Circuits: Modeling, Design, Testing	**C4L-C** Algorithms and Processors	
18:20	ROOM Sevilla I - CLOSING CEREMONY (Prof. Ángel Rodríguez-Vázquez)			

COMMITTEES

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WELCOME TO SEVILLA

Seville ("Sevilla" in spanish), rich millenary heiress of different cultures that settled along the shores of the Guadalquivir River, preserves and pampers its world famous monumental architecture. At the same time it proudly and brilliantly treasures mysterious secrets that romantic authors attempted to release in mythical works such as Carmen, The Barber of Seville or Don Juan, amongst many others.

Nonetheless, the Seville that we wish to introduce to you today is a synopsis of the values of its past heritage and modernity of its present reality. Such a symbiosis holds the city's historical character which offers contemporary infrastructures which convert the city into a first class tourist destination, not just for the individual tourist but also for the business person attending conferences or incentive trips.

THE CATHEDRAL AND THE GIRALDA

"Let us create such a building that future generations will take us for lunatics". That's what churches authorities repudetly agreed back in 1401. And they certainly got themselves the big and magnificent Cathedral, one of the largest catholic churches in the world: the main building is 126m long and 83m wide. The original mosque's beautiful minaret (for the cathedral was built over the main mosque that fell to the christians in 1248), La Giralda, still stands on its eastern side, but the cathedral's bulky exterior gives few other hints of the treasures within.

Price per person: €7.50
Hours: Mon-Sat: 11:00 - 17:00
Phone: (+34) 954 214 471

ALCÁZAR

Residence of many generations of kings and caliphs, the not-to-be-missed Alcázar is an intriguing, beautiful complex of gardens, patios, and royal rooms, and it is intimately associated with the lives and loves of many Muslim and Christian rulers, above all Pedro I of Castilla, who was known as Pedro El Cruel and Pedro El Justiciero (the Cruel and the Justice-dispenser) depending which side of him you were on.

Price per person: €7
Hours: Thu-Sat: 09:30 - 17:00. Sun: 09:30 - 13:30
Phone: (+34) 954 502 324

SANTA CRUZ, THE CENTRO, AND THE ARENAL

Santa Cruz is Seville's medieval Judería (Jewish quarter), today a tangle of quaint, winding streets and lovely plant-decked plazas perfumed with orange blossom. Plaza de Santa Cruz, Plaza Doña Elvira, the 17th-century Hospital de los Venerables Sacerdotes, are spots the visitor won't want to miss here. The real center of Sevilla, El Centro, is densely packed with narrow streets and broken up by squares and streets (Calle Sierpes, Casa Pilatos, Plaza del Salvador, ...) around which the city's life has revolved for aeons. The Arenal, a short walk from the Cathedral, brings the visitor to the Río Guadalquivir. Seville's most interesting sights here include the Torre del Oro (a 13th-century islamic watch tower), Plaza de Toros (the bullring, one of the most handsome in Spain and probably the oldest), the Hospital de la Caridad and the Museo de Bellas Artes (Fine-Arts Museum), which is the second Art Gallery in the country.

CLIMATE

Seville has a Mediterranean weather due to the oceanic influences nearby. In the winter the temperatures are mild, and in the summer the weather is hot. Precipitation varies along the year, concentrated in the period October to April. December is the wettest month, and the coldest are January and February. June, July, and August are the hottest months.

FAST FACTS

Country: Spain / España
Status: city / capital of Andalusia
Population: 720,000 in the city + another 400,000 in its outskirts
Language: Spanish

WELCOME TO SEVILLA

Time zone: UTC+2 at summer time (March 28 to October 31), UTC+1 at winter time (From October 31)
Country dialling code: +34
Telephone area code for Seville: 95
Currency: Euro is the official currency of Spain. Euro (€) = 100 cents. Notes are in denominations of €500, 200, 100, 50, 20, 10, and 5. Coins are in denominations of €2, €1, and 50, 20, 10, 5, 2, and 1 cents. Money can be taken from cash machines (ATMs) which accept most international cards.
Health and security:
- **Emergency service** (Fireman, police, civil protection, sanitary emergency) phone number: 112
- **National police:** emergency telephone number: 091
- **Local police:** emergency telephone number: 062
- **Medical emergencies:** emergency telephone number: 061

Tipping: tipping in Spain is not obligatory but it is common to leave some change or to give a tip of 5–10%. There are no added service charges on the final bill at any hotel, restaurant, or bar.
Electricity: 220 volts, 50 Hz - round two-pin plugs are used
Measures: Weight measured in kilograms, distances measured by the metric system, temperature measured in degrees Celsius
Tourism: Over 2 million tourists visit Seville Province each year.
Tourist Office: Paseo de las Delicias, 9 (Costurero de la Reina) 41012 Sevilla. Phone: +34 954 234 465
Seville tourism information can be found at:
www.turismosevilla.org, www.andalucia.org

PHARMACIES

A chemist's or drugstore is known as a Farmacia and they can be identified by a large green or red cross sign outside. They tend to keep the same working hours as other shops and if closed, usually display a sign indicating the nearest pharmacy that is open. As well as selling prescription medicines, they also offer free advice about minor injuries or ailments and they will happily suggest non-prescription treatments. Usually open from 9.30am to 1.30pm, and from 4.30am to 8.00pm. Besides you can find pharmacies that open 24 hours. Pharmacies follow a rolling late-hour schedule, which is published in the newspapers and the internet, and is posted at all pharmacies.

OPENING HOURS FOR BUSINESS/SHOPS IN SEVILLE

Most offices in Seville open at 9.00am and many close for a couple of hours in the afternoon, although this varies with companies. The most common business time-table is from Monday to Friday, from 9.30am to 1.30pm, and from 5.00pm to 8.00pm. Many shops also open on Saturdays from 9.30am to 1.30pm. Big shopping centers and department stores open

from 10.00am to 9.00pm or 10.00pm uninterruptedly, except Sundays and local holidays.

Opening Hours for Banks

Banks are generally open Monday-Friday from 8.30am to 2.00pm, and sometimes on Saturday from 8.30am to 1.00pm.

Currency Exchange

There are many places to exchange currency, the banks being the ones with best rates. There are also foreign exchange outlets in the airports and even in some hotels and restaurants, although the rates are usually not so favourable. Withdrawing money at a cash point (ATM) is often the most convenient and economic way to obtain Euros and there are ATMs all over the city. Many are located inside banks or in their facades.

Credit Cards, Travellers Cheques

Credit cards are widely accepted at establishments throughout Seville and these include Visa, EuroCard, Access, MasterCard and American Express. In some stores, you may be asked to enter your PIN (Personal Identification Number) into a keypad for security purposes. Some shops do not accept credit card payment for a small monetary amount. Travellers cheques, accompanied by a passport, are also accepted in most hotels, restaurants, and shops.

ATMs (Automatic Teller Machine)

There are ATMs almost everywhere, and most support Visa/ Plus, Cirrus, and other popular systems. Just look for the signs next to the ATM or on the display itself. ATMs are easy to use here and all offer English as well as other languages.

VAT Refund

How to get IVA (VAT) back on shopping: If a buyer's residence is outside the European Union, then he/she can claim back the tax on purchases, as long as they amount for more than €90.15 in each establishment. In order to do so, you should ask for a tax-free receipt, wherever you see the Spain Refund Tax-free Shopping logo, at the point of sale. The Tax-Free cheque must be stamped, always before the check-in. Show the goods to customs when leaving the country. You can claim your money in the SPAIN REFUND cash agents in airports and borders.

Currency Choice Logo

The Currency Choice logo next to a credit card terminal means that there you can pay by credit card in your own national currency. The amount on the receipt is the sum that will be debited to your bank. No hidden fees, no surprises when you get back home.

WELCOME TO SEVILLA

VISA INFORMATION

Anyone wishing to travel to and enter Spain must have a valid passport and/or the appropriate Spanish Visa. We recommend contacting your local Spanish consulate or Embassy for more information on these requirements.

For further information about Sevilla, please check
www.infosevilla.com

The conference will be held at the:

BARCELÓ RENACIMIENTO HOTEL

Isla de la Cartuja, s/n
E-41092

The avant-garde Barceló Renacimiento***** is a modern, top-quality hotel located in Seville, on the Island of La Cartuja, on the banks of the Guadalquivir river, that is today home to the Cartuja scientific and technologic park. It is the best equipped hotel in the city to accommodate groups, conferences, congresses, and incentive trips, boasting its own 25-room Convention Center.

Conveniently located, just a few minutes away from Seville's historic center, the high-speed AVE train station and the airport close by, is an attractive option for both business travelers and people interested in urban sight-seeing.

Barceló Renacimiento's facilities include 25 meeting rooms and 2 atriums for events. The Convention Center Gran Sevilla was opened in 2002 and it provides fully equipped 1,024m^2 ideal for any kind of event. It can be turned into 3 independent rooms where natural light is very important. Besides, there is an exhibition area of 800m^2.

Barceló Renacimiento hotel is member of the International Congress and Conventions Association (ICCA).

LOCATION

COORDINATES: LAT: 37° 24' 35" N
LONG: -5° 59' 43" W - E

CONFERENCE VENUE

A range of hotels (see map below) to suit all budgets and requirements are also within a short distance of the meeting venue.

How to Reach the Venue

Strategic location with an easy access, in a few minutes, both to the city's historical center and to the AVE train station or the airport.
Distance to the city center: 1-2 km.
Distance to the airport: 10 km.
Train station: 20 min.

BY BUS

There is a good service city buses from/to the most important parts of the city, which takes around 10-20 minutes. Walking distance to bus stop: 3-5 minutes.
Please, see below section "Getting around" for further information.

BY TAXI

Taxi stops are located on several central streets and squares. Taxis, though, can be hailed any place in the city when they show the "libre" (free) sign or a green light. From 7.00am to 9.00pm Monday to Friday, taxis cost around €1.26 plus €0.87 per kilometer. At other times and on public holidays, it's €1.53 plus €1.07 per kilometer.
Taxi Phones: 954 675 555, 954 580 000, 954 622 222
www.taxisevilla.es, www.taxigiralda.es

RAILROAD/RAILWAY

The railroad transportation system connects all major urban centers. The **Santa Justa train station** serves as an important hub for connections between the Andalusia's main cities and all of the autonomous regions of Spain and Europe.

AVEs (high speed trains) connect to/from Cordoba (around €34 to €60, 40 minutes), Malaga (€23 - €45, 2½ hours), Madrid (€85 - €160, 2½ hours) or Barcelona (€145 - €260, 5½ hours).

In addition to the AVE service, this modern station concentrates all railway traffic, with trains to various towns of the province, to all the capitals of Andalusia and to other Spanish cities such as Valencia, Alicante, and Cáceres.

The **Santa Justa Train Station** is located at Avda. Kansas City s/n. 41007 Sevilla, Information phone +34 902 320 320. International information phone: +34 902 243 402

For further information about train services and other train types and destinations please visit the website at www.renfe.es

ROADS

Highway and access roads and rapid beltways provide precise connections to all neuralgic points of the city and its surroundings. Seville has now become one of Spain's best connected cities by road, with highways connecting all Andalusia's main cities as well as Madrid and Portugal. Main access roads are the A-92, N-IV, A-4, and A-49.

GETTING AROUND

City Buses:

(Spanish name: *autobús*) Buses are the cheapest way to get around Sevilla. A single bus ride is €1.20, but you can buy a voucher with 10 trips (*bonobús*) from €7 at a newsstand or tobacco shop. The city bus network is based around four lines- C-1, C-2, C-3, and C-4- which follow circular routes, linking the main transport terminals and the city center. Four transversal lines and a series of radial lines which lead into the center from the four points of the compass complete the bus network.

You can pick up a bus route map, *the Guía del Transporte Urbano de Sevilla*, from tourist offices or from information booths at major stops (including Plaza Nueva, Plaza de la Encarnación and Avenida de Carlos V).

Information Phone: 010 (press 5) Web Site: www.tussam.es

On the other hand, Seville has two bus stations, each providing services to separate cities:

- **Prado de San Sebastián**, just southeast of the Barrio de Santa Cruz, provides bus services to cities of Andalusia. Address: Manuel Vázquez Sagastizábal, s/n. Sevilla. Phone: +34 954 417 111

CONFERENCE VENUE

- **Plaza de Armas**, by the Cachorro's bridge, connects with the rest of Spain, the Province of Huelva, and Portugal. Address: Avenida del Cristo de la Expiración, s/n. - Sevilla. Phone: +34 954 908 040

Sightseeing tour buses:

Tour buses can be a great way to get around Seville. You have the option of traveling the full circuit and getting an overview of what to expect in the city or get on and off as many times as you want, seeing the sights as you go.

Web site: www.busturistico.com

Taxis:

Taxi stops are located on several central streets and squares. However, taxi can be hailed any place in the city when they show the *libre* (free) sign or a green light.

Many of the short cab rides cost between 3-6€. From the airport to the city center or the opposite there is now a flat rate. The fee is €21.89 during the day and €24.41 during holidays, Sundays or night (after 10pm).

Phones: +34 954 675 555 / +34 954 580 000 / +34 954 622 222

Web sites: www.taxisevilla.es, www.taxigiralda.es

Subway and tram:

(Spanish name: *metro*) Seville's subway system has only one line that goes from the west to the south part of the city and surrounding suburbs. A single ride is €1.30.

(Spanish name: *tranvía metro centro*) (T1) is a surface tram by the center of Seville that connects Plaza Nueva to Prado de San Sebastián bus station, with a total of 1.3km. This route covers the pedestrian area in the city center.

Web site: www.metrodesevilla.org

Bicycle:

(Spanish name: *bicicleta*) Sevici is the name of a community bicycle program in Seville. Its purpose is to cover the small and medium daily routes within the city in a climate friendly way. More than 250 stations and 2500 bikes will be available. The stations are situated throughout the inner-city with a distance of around 200 meters between each one, with many situated next to public transport stops to allow for intermodal use. The bikes can be borrowed from, and returned to, any station in the system, making it suitable for one way travel. Each station has between 10 and 40 parking slots to fix and lock the bicycle.

There is a short term subscription for tourists with an unlimited number of journeys during 7 consecutive days (a deposit of €150 is mandatory).

Web site: www.sevici.es

Other ways:

On foot: The city center of Seville is not very large and it is easy to walk to all the tourist spots, a lot of fun to walk around. The center has almost become completely car-free.

Horse-Drawn carriage tour: it is very typical way to get around Seville.

River cruises along the Guadalquivir River: the emblematic Andalusian river, the Guadalquivir is the only navigable river in Spain.

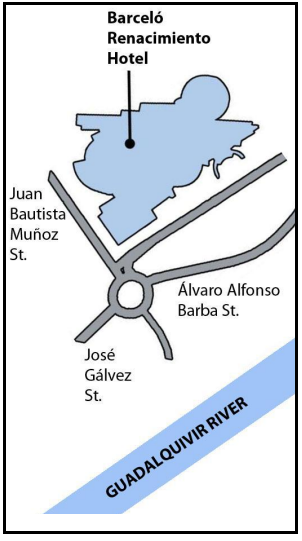
Sevilla Tourist Card

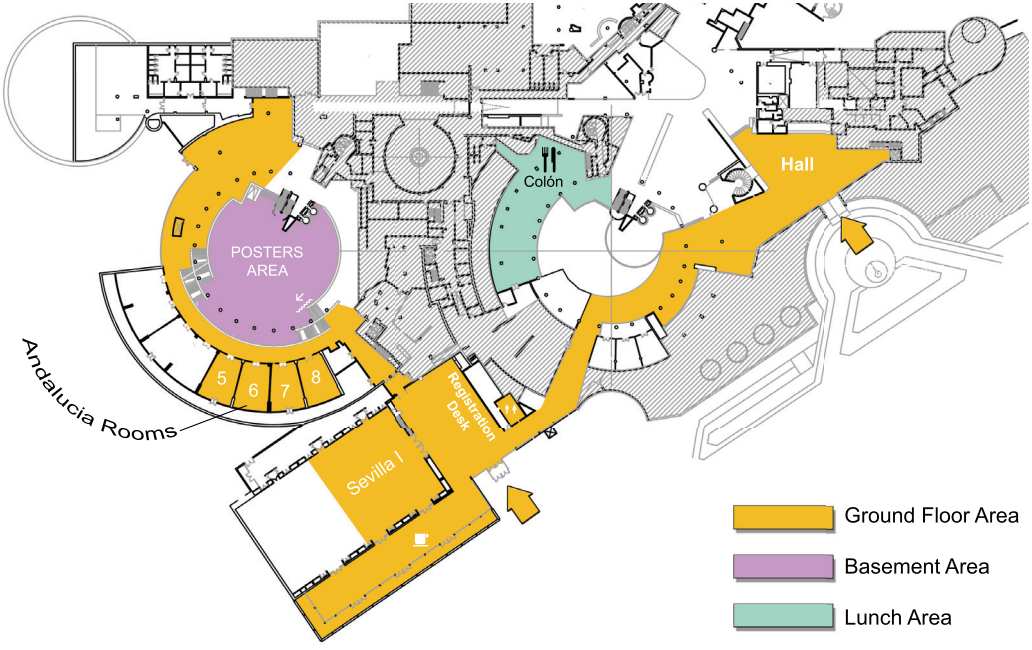
Sevilla Card, the Seville tourist card, will help you discover the city and enjoy your stay and save money. Its price is from €32. Some advantages with the card are:

- Free admission to most museums and monuments in the city and environs.
- Unlimited use of sightseeing buses.
- Boat rides on the Guadalquivir River.
- *Isla Mágica* Theme Park.
- Besides you will be able to enjoy discounts in shops, restaurants, shows, and leisure centers for adults and children.
- Guide/map with information about museums, services included, and participating establishments.
- A free “traditional tapa” as well as a drink.

Web site: www.sevillacard.es

CONFERENCE VENUE





CONFERENCE VENUE

CONFERENCE INFORMATION

LANGUAGE

The official language of the meeting is English.

WEBPAGE

ICECS 2012 webpage: **www.ieee-icecs2012.org**

REGISTRATION DESK

Sunday, December 9th, 2012:	08:30 - 14:30
Monday, December 10th, 2012:	07:15 - 17:00
Tuesday, December 11th, 2012:	08:00 - 17:00
Wednesday, December 12th, 2012:	08:00 - 17:00

NAME BADGES

All participants and accompanying persons are asked to wear their name badges in a visible place. Entrance to sessions is restricted to registered delegates only. Entrance to meeting halls, poster and exhibition areas is granted to badge holders.

SPEAKERS BRIEFING

A digital projector and a PC are available in all conference rooms. Speakers should upload their presentations in advance at the Conference Registration Desk with the help of technical staff. ICECS Organization recommends speakers to use the computers in the conference rooms, which have installed Windows 7 OS with Windows Power Point 2010 and Adobe Acrobat PDF Reader. All presentation files will be deleted at the end of the conference and no copy will be saved.

The time scheduled for each presentation is about 17 min for lectures and 3-4 min for poster briefing. Questions to the authors are very welcome and can be raised at the end of the presentation or at the end of the session, according to the chairman's decision. Chairmen and speakers are requested to respect scheduled times. Authors should meet their chairman in the session room 15 min ahead the respective sessions.

Speakers are kindly requested to present a short bio at the Conference Registration Desk the day of arrival. This information is useful for the chairman to correctly introduce the speaker of the paper.

INTERNET ACCESS

Wireless internet access will be available at the conference venue without charge. More info will be provided at the Conference Registration Desk.

CONFERENCE PROCEEDINGS

All participants will receive an electronic copy of the ICECS 2012 Proceedings in a USB flash drive.

BEST PAPER AWARD

Papers presented at the conferences will be considered for the Best Paper Award. The jury will be composed by members of the

CONFERENCE INFORMATION

Organization Committee and of the Technical Program Committee. The award delivery will take place during the closing ceremony.

INSURANCE DISCLAIMER

Participants are responsible for their own insurance. The organizers cannot take responsibility for any accident, loss or damage to participants or their property during the event.

COMPLAINTS

While we hope that your time at the conference is enjoyable, if you encounter a problem during your stay, please report it to the registration desk as soon as possible. The conference team will make every effort to rectify the issue.

MEALS AND REFRESHMENTS

All meals and refreshments will be served at scheduled times during the conference program.

MONDAY, DECEMBER 10TH, 2012

Morning refreshments	In front of Room Sevilla I
Lunch	Colón
Afternoon refreshments	In front of Room Sevilla I
Welcome Reception	Hotel Barceló

TUESDAY, DECEMBER 11TH, 2012

Morning refreshments	In front of Room Sevilla I
Lunch	Colón
Afternoon refreshments	In front of Room Sevilla I
Gala Dinner*	Abades Triana Restaurant

WEDNESDAY, DECEMBER 12TH, 2012

Morning refreshments	In front of Room Sevilla I
Lunch	Colón
Afternoon refreshments	In front of Room Sevilla I

*The Gala dinner is included in the registration conference fee. To buy additional tickets, please contact the registration desk.

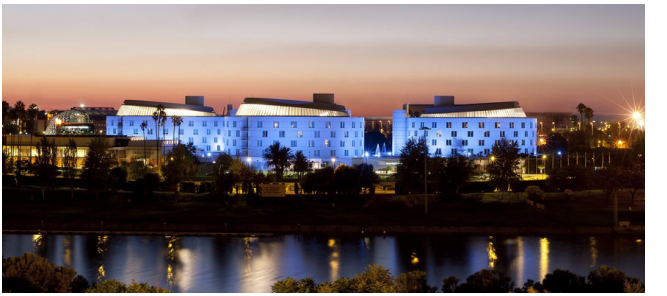
Participants with special dietary requirements who have not previously informed about it please contact to the registration desk in order to provide an alternative menu.

SOCIAL PROGRAM

MONDAY, DECEMBER 10TH, 2012

WELCOME COCKTAIL

The Welcome Cocktail will take place at Hotel Barceló (conference venue) on December 10th, at 19:30.



A hotel with a unique beauty, set on three circular buildings or atriums surrounded by gardens, open spaces, and an incomparable Guadalquivir river view.

Barceló revival has become an essential reference in Seville for holding conventions, conferences, and all kind of international events.

Don't miss this opportunity to know your fellow participants to the Conference ICECS 2012. Enjoy it!

TUESDAY, DECEMBER 11TH, 2012

GALA DINNER

The Gala Dinner program will include a panoramic city sightseeing tour and a visit to the Alcázar.

The local organization will provide buses for the transportation from Hotel Barceló. We will leave the conference venue from 19:30 to 20:00. Attendees who prefer, can join us at the door of the Lions (Puerta de los Leones), in the Alcázar at 20:00.

Seville is the artistic, cultural, and financial capital of the southern Spain. The city is a historical masterpiece full of Islamic monuments, gardens, and flamenco festivals.

We will begin our city sightseeing tour from Hotel Barceló, with a view of the most relevant monuments and sights of the city.

After that, we will visit the Alcázar, also called Real Alcázar or Reales Alcázares de Sevilla. This beautiful place began to take its present form after the conquest in 713 of Seville by the Arabs, who used Alcázares as the residence of its leaders from 720. After the Reconquista in 1248, it was the accommodation of King Fernando III, taking on the habit of lodging the successive monarchs.

It is now used as a place of accommodation for members of the Royal Family and dignitaries who visit the city. The important events that take place in the city are often held in the Alcázar. The Alcázar and its gardens are one of the main attractions of the Seville.

The Gala Dinner will be held at Abades Triana Restaurant.

An exquisite place, located in Triana's heart, in front of the Golden Tower (Torre del Oro), where you can enjoy the best dinner and the Guadalquivir river views.

Finally, we will return to Hotel Barceló for resting.

OPTIONAL LEISURE ACTIVITIES

Sightseeing Tours and Activities

You have the opportunity to make different sightseeing tours and activities offered at a reduced price for ICECS attendees. To register and get more information, please visit http://www.ieee-icecs2012.org/registro/activities/registration_form.php

Activities (December 8-12, 2012)

Sevilla Alcázar, El Salvador (guided morning tour)

Departure Days: Sunday, Wednesday, Friday
Duration: 3½ hours
Departure Point: Hotel or place assigned by the agency
€37 Tax Included

Sevilla Cathedral, Giralda Tower, and Basílica Macarena (guided morning tour)

Departure Days: Monday, Tuesday, Thursday, Saturday
Duration: 3½ hours
Departure Point: Hotel or place assigned by the agency
€37 Tax Included

Sevilla Bullring and River Cruise (guided afternoon tour)

Departure Days: Sunday, Monday, Wednesday, Friday
Duration: 3 hours
Departure Point: Hotel or place assigned by the agency
€32 Tax Included

Monumental Sevilla (morning tour)

Departure Days: Saturday, Monday, Tuesday, Thursday
Duration: 3 hours
Departure Point: Main door of the Starbucks cafe - San Fernando Street 1 (Puerta Jerez)
€22 Tax Included

Typical Sevilla

Departure Days: Sunday, Wednesday, Friday
Duration: 3½ hours
Departure Point: Main door of the Starbucks cafe - San Fernando Street 1 (Puerta Jerez)
€29 Tax Included

Roman City of Itálica (afternoon tour)

Departure Days: Saturday, Tuesday, Thursday
Duration: 4 hours
Departure Point: Hotel or place assigned by the agency
€29 Tax Included

Noche Sevillana

Departure Days: Daily

OPTIONAL LEISURE ACTIVITIES

Duration: 3 hours
Departure Point: Hotel or place assigned by the agency
€50 Tax Included

Tickets River Cruise + Flamenco Show (afternoon)
Departure Days: daily
Duration: 3 hours
Departure Point: Boat: Muelle Torre del Oro / Flamenco: María Auxiliadora Avenue 18 B
€45 Tax Included

Tickets River Cruise + Flamenco Show (night)
Departure Days: daily
Duration: 3 hours
Departure Point: Boat: Muelle Torre del Oro / Flamenco: María Auxiliadora Avenue 18 B
€45 Tax Included

Córdoba
Departure Days: Saturday, Tuesday, Thursday
Duration: 9 hours
Departure Point: Hotel or place assigned by the agency
€95 Tax Included

Jerez & Cádiz
Departure Days: Tuesday, Thursday
Duration: 9 hours
Departure Point: Hotel or place assigned by the agency
€105 Tax Included

Hop On Hop Off Tour Bus
Departure Days: Daily
Duration: 24 hours
Departure Point: Torre del Oro
€16 Tax Included

Sevilla Walking Tour + River Cruise
Departure Days: Daily
Duration: 2½ hours
Departure Point: Torre del Oro
€32 Tax Included

Walking Tour + Horse-Drawn Carriage Tour
Departure Days: Daily
Duration: 2½ hours
Departure Point: Plaza de España
€54 Tax Included

Romantic Sevilla
Departure Days: Daily

Duration: 2 hours
Departure Point: Plaza de España
€85 Tax Included

MUSEUMS IN SEVILLE

Free entry for EU citizens. Non-EU citizens: €1.50 to the following museums:

- Museo Arqueológico de Sevilla (**Archaeological Museum**)
  www.museosdeandalucia.es/cultura/museos/MASE/?lng=en
- Museo de Bellas Artes (**Museum of Fine Arts**)
  www.museosdeandalucia.es/cultura/museos/MBASE/?lng=en
- Museo de Artes y Costumbres Populares (**Museum of Arts and Traditions**)
  www.museosdeandalucia.es/cultura/museos/MACSE/
- Conjunto Arqueológico Itálica (**Archaeological Ensemble Italica**)
  www.museosdeandalucia.es/cultura/museos/CAI/
- Conjunto Arqueológico de Carmona (**Archaeological Ensemble Carmona**)
  www.museosdeandalucia.es/cultura/museos/CAC/?lng=en

Non-free entry:

- Monasterio de la Cartuja (**Cartuja Monastery)** and Centro Andaluz de Arte Contemporáneo (**Andalusia Contemporary Art Center**)
  www.juntadeandalucia.es/cultura/caac/english/frame.htm
  €1.80 Visit the monument or to the temporary exhibitions
  €3.01 Complete visit

MONDAY, DECEMBER 10TH, 2012

ULTRA-LOW-POWER CIRCUIT TECHNIQUES FOR IMPLANTED/MEDICAL APPLICATIONS

Prof. Yusuf Leblebici
Director of the Microelectronic Systems Laboratory at the École Polytechnique Fédérale de Lausanne (EPFL)

Prof. Yusuf Leblebici received the B.Sc. and M.Sc. degrees in electrical engineering from Istanbul Technical University, Istanbul, Turkey, in 1984 and 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign (UIUC), in 1990.

Between 1991 and 2001, he worked as a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI). In 2000-2001, he also served as the Microelectronics Program Coordinator at Sabanci University. Since 2002, he has been a Chair Professor at the Swiss Federal Institute of Technology in Lausanne (EPFL), and director of Microelectronic Systems Laboratory. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is the coauthor of four textbooks, namely, *Hot-Carrier Reliability of MOS VLSI Circuits* (Kluwer Academic Publishers, 1993), *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), *CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications* (Springer, 2007) and *Fundamentals of High Frequency CMOS Analog Integrated Circuits* (Cambridge University Press, 2009), as well as more than 200 articles published in various journals and conferences.

Dr. Leblebici has served as an Associate Editor of IEEE Transactions on Circuits and Systems II and IEEE Transactions on VLSI Systems. He has also served as the general co-Chair of the 2006 European Solid-State Circuits Conference, and the 2006 European Solid State Device Research Conference (ESSCIRC/ESSDERC). He has been elected as Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010-2011 and is an IEEE Fellow.

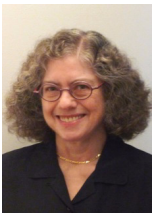
PLENARY LECTURES

TUESDAY, DECEMBER 11TH, 2012

FROM DATA TO INSIGHT

Dr. Ellen J. Yoffa
Director, Information & Interaction
IBM T. J. Watson Research Center
Yorktown Heights, New York, USA

Abstract
In our daily lives, we're surrounded by massive amounts of rich multimedia data of all kinds. The challenge is to interpret this data and use it to make intelligent decisions in real time. In this talk, I'll highlight a selection of projects from the Information & Interaction team at IBM Research. These projects explore technologies for human language understanding, image processing, and social network analysis. This research aims to extract insight from the data around us.



Dr. Ellen J. Yoffa is Director of Information & Interaction at the IBM T. J. Watson Research Center. She leads research in a spectrum of technologies from mobile to human language and image analytics to social networking. She is past President of the IEEE Circuits and Systems Society and currently serves on several IEEE committees, including the Technical Activities Strategic Planning Committee, TAB Financial Committee and the IEEE Ethics & Member Conduct Committee, and has been elected to the 2014 IEEE Board of Directors. She received the 2009 IEEE Circuits and Systems Society Meritorious Service Award. Dr. Yoffa spent many years in electronic design automation research and chaired the 1997 IEEE/ACM Design Automation Conference. She was awarded the 2006 Marie R. Pistilli Achievement Award for Women in Electronic Design Automation. She received a BS and PhD in Physics at the Massachusetts Institute of Technology and is an IEEE Fellow.

WEDNESDAY, DECEMBER 12TH, 2012

COMPRESSED SENSING ANALOG-TO-DIGITAL CONVERSION

Prof. Michael P. Flynn
Dept. of Electrical Engineering & Computer Science (EECS) at the University of Michigan

Abstract
The amount of digital information in the world has increased dramatically over the past few years. As the portability and computing power of electronics has improved a need for both high-capacity data storage centers and large wireless communication infrastructures has arisen. However, the transmission of data often dominates the energy consumption in portable electronics. Although technology scaling has reduced the energy cost per transistor in digital circuits, and has improved the overall energy efficiency of digital computing, the energy cost associated with data communication still dominates. In order to match pace with the available computing resources, the energy efficiency of data transmission must improve. In addition, the energy efficiency of data acquisition through analog-to-digital conversion must also improve to support the growth in digital information processing. Compressed sensing promises to improve the energy efficiency of sensing systems, and of wireless communication and analog-to-digital conversion. This lecture reviews the concepts behind compressed sensing and surveys some recent approaches to compressed sensing in analog to digital conversion.

Prof. Michael P. Flynn received the Ph.D. degree from Carnegie Mellon University in 1995. From 1988 to 1991, he was with the National Microelectronics Research Centre in Cork, Ireland. He was with National Semiconductor in Santa Clara, CA, from 1993 to 1995. From 1995 to 1997 he was a Member of Technical Staff with Texas Instruments, Dallas, TX. During the four-year period from 1997 to 2001, he was with Parthus Technologies, Cork, Ireland. Dr. Flynn joined the University of Michigan in 2001, and is currently Professor.

Michael Flynn is a 2008 Guggenheim Fellow. He received the 2011 Education Excellence Award and the 2010 College of Engineering Ted Kennedy Family Team Excellence Award from the College from Engineering at the University of Michigan. He

received the 2005-2006 Outstanding Achievement Award from the Department of Electrical Engineering and Computer Science at the University of Michigan. He received the NSF Early Career Award in 2004. He received the 1992-93 IEEE Solid-State Circuits Pre-doctoral Fellowship. He is an Associate Editor of the IEEE Journal of Solid State Circuits (JSSC) and serves on the Technical Program Committees of the International Solid State Circuits Conference (ISSCC) and the IEEE Symposium on VLSI Circuits. He formerly served on the program committee of the Asian Solid-State Circuits Conference was Associate Editor of the IEEE Transactions on Circuits and Systems II from 2002 to 2004.

TUTORIAL 1

ADVANCES IN TIME-ENCODED ANALOG SIGNAL PROCESSING AND DATA CONVERSION

Luis Hernandez, Susana Paton, Enrique Prefasi
Electronics Department of Carlos III University, Madrid, Spain

Pieter Rombouts
Electronics and Information Systems Department of Gent University, Belgium

Sunday, December 9th, 2012 (9:00 - 13:00)
Room Andalucía 5

Abstract

The feature size improvement of nanometer CMOS technology represents an enhancement of speed and power consumption for digital circuits but at the expense of analog performance degradation. Time encoding techniques are one of the research trends in analog signal processing to overcome this problem and ease an accurate representation of analog signals within nanometer CMOS chips operating at very low voltage. In essence, time encoding techniques map a continuous time signal into a pulse coded signal. As long as pulse streams are formed of discrete events, some signal processing concepts are needed to bridge both kind of representations. Most time encoding techniques used so far stem from classical pulse modulations such as PWM, PPM and from non uniform sampling schemes. These techniques are known from a signal processing point of view since long ago, but its particular application may not be familiar to analog circuit designers. This tutorial will explore the basics of time encoding techniques and especially, its application to data conversion.

An introductory presentation will review the signal processing concepts involved in time encoding techniques and its implications when applied to CMOS circuit design. A second presentation will discuss the design of continuous time sigma delta converters that rely on time encoding to replace multibit internal ADCs and DACs. This presentation will cover both system and circuit level aspects. Finally, we will show the recent advances in time encoded signal processing using mostly digital elements such as gated and voltage controlled ring oscillators, variable delay gates and asynchronous digital circuitry.

Topics

- Introduction to Time Encoded Signal Processing (P. Rombouts)

TUTORIALS

- Design of Continuous Time Sigma Delta Modulators with Time Encoded Quantizers (S. Paton)
- CMOS Circuit Design for Time Encoded Analog Signal Processing (E. Prefasi)
- Time Encoded Signal Processing Using Mostly Digital Circuitry (L. Hernandez)

TUTORIAL 2

SILICONIZED PHOTONICS-ELECTRONICS AS AN EMERGING TECHNOLOGY

Henry H. Radamson, Lars Thylén
KTH Royal Institute of Technology, Sweden

Sunday, December 9th, 2012 (9:00 - 13:00)
Room Andalucía 6

Abstract
Silicon photonics is an emerging technology offering novel solutions in different areas such as optical communications, optical computer interconnects, sensing, bio-applications, all requiring highly integrated novel photonics-electronics. Silicon photonics-based communication has many advantages over electric wires for multiprocessor and multicore macro-chip architectures including high bandwidth data transmission, high speed and low power consumption, not possible with all electronics solutions at the required high transmission rates. Following the INTEL's concept to "siliconize" photonics, silicon device technologies should be able to meet the requirements for six main building blocks for realization of the emerging optical interconnects technology: light generation, guiding of light including electronically controllable wavelength selectivity, light modulation for signal encoding, detection, low cost assembly including optical connecting of the devices to the real world and finally the electronic control systems.
The silicon-based materials, mainly alloying Si with other elements in the group IV, in form of quantum well or dot structures demonstrate new photonic properties as well as carrier transport, paving the path for a paradigm shift which is along with the semiconductor industry's needs in the near future. For example, novel Sn-GeSi materials have shown the possibility of having direct bandgap property. Epitaxial growth of strained (or relaxed) Sn-GeSi materials on Si for lasing and detection of telecommunication wavelengths is an on-going development.

This tutorial includes the all important issue of light generation and detection in group IV materials, an overview of waveguide silicon photonics devices, including the possibility of employing the silicon compatible electro-optic polymers for high speed, low power phase modulation, especially important in view of the quest for advanced modulation formats and then presents how this photonics technology can be developed into a monolithically integrated photonics-electronics technology on silicon, which can be obtained when Sn-GeSi alloys are integrated in the chip. The tutorial will also present briefly the CMOS part of the chip in the *More than Moore* approach of the roadmap. The difficulties to achieve the next technology node (16 nm node by 2014 timeframe) will be shortly overviewed. The future down-scaling of transistors is discussed, when the *quantum tunneling* will occur and limits the functioning of devices (no matter of the applied material). This tutorial will provide insights into a potential Si electronics-photonics roadmap scenario when new material systems and concepts are introduced.

Topics

- Building lasers and detectors from group IV materials (H. Radamson)
- Modulators, switches and WDM devices: Plasmonics and electrooptic polymers for Si based low power nanophotonics integrated photonics fabrics for communications and interconnect (L. Thylen)
- Merging the best of two worlds: Issues in monolithic nanoscale photonics-electronics integration (H. Radamson)

TUTORIAL 3

RF CMOS Wireless Receivers for 402MHz Medical Implantable Communication Systems

Sherif Mohamed, Yiannos Manoli
Fritz Huettinger Chair of Microelectronics, IMTEK
Albert-Ludwig-University Freiburg

Sunday, December 9th, 2012 (9:00 - 13:00)
Room Andalucía 7

Abstract

With the increasing number of portable and implantable personal health care devices, there is a strong demand to

control their communication in a single wireless network. The advances of the communication technologies have made these devices easier to use. One of the problems which render the using of these devices is the power consumption. There are wireless and wireline approaches to implement the BSN network. Recently, wireless body-area-network (WBAN) is getting more and more attention. WBAN is composed of numerous healthcare devices or physiological sensors and also provides wireless connectivity among them for the continuous and ambulatory health care. WBAN technologies have been an active research area, and it is categorized into wearable BAN and implantable BAN. The wearable BAN is only for communication among the on-body devices such as electrocardiogram (ECG), electroencephalography (EEG), electromyography (EMG), and body temperature sensors. On the other hand, the implantable WBAN connects the implanted devices such as pacemaker with on-body controller.

For the data transmission with implanted medical devices, the 402-405 MHz, medical implant communication service (MICS) Transceivers, NB PHY, is adapted for the in-body devices. MICS standard is divided into 10 channels for listen-before-talk (LBT) protocol as mainly discussed by Federal Communications Commission (FCC). This needs 10ms for scanning the channel before each MICS communication starts.

Topics

- A fully monolithic CMOS direct conversion and low-IF receiver architecture with integrated quadrature LO chain, which implemented in a closed-loop type-II PLL system for 402-405MHz band (MICS applications). This system are designed and implemented in a 0.13-μm CMOS process.
- Design of a dual-band wireless communication system that can communicate in/on-sensors of the human body for BSN network. The transceiver system support the 30- 70MHz BCC and 402-405MHz MICS standards. The key future of the dual-system is that the BCC system is utilized during the scan period of the MICS channel, which results in reducing the system power consumption.
- This tutorial is also focusing on designing and implementing an ultra-low power super-regenerative transceiver that employs improvement in amplitude-shift keying or applying frequency-shift keying for flexible date rates without the need for expensive off-chip components.

TUTORIAL 4

DIGITAL DELTA-SIGMA MODULATORS FOR DAC AND FRACTIONAL-N FREQUENCY SYNTHESIS APPLICATIONS

Michael Peter Kennedy
Department of Electrical & Electronic Engineering and Tyndall National Institute, University College Cork, Ireland

Sunday, December 9th, 2012 (15:00 - 19:00)
Room Andalucía 5

Abstract
Delta-Sigma Modulation (DSM) is increasingly used in digital to analog converters and frequency synthesizers. Classical analysis of DSM makes assumptions about quantisation that promote linear ways of thinking. Many of the unexpected phenomena that degrade the performance of real systems are due to underlying nonlinear effects. The use of finite state machines adds a further level of complexity. This tutorial is in four parts. Part I addresses ideal Digital Delta- Sigma Modulator (DDSM), explains what signal processing assumptions are commonly made to understand its operation, and presents an overview of applications of DDSMs. Part II focuses on the real DDSM, identifying what can go wrong and why. Part III presents state of the art solutions to problems that result from nonlinearities and finite states. The key issue addressed is spurious tones: how they arise and how to eliminate them. Part IV addresses complexity reduction strategies facilitated by error-masking.

Topics

- The ideal Digital Delta-Sigma Modulator—what you learn in school.
  Architecture and governing equations. Signal processing assumptions. Applications of DDSMs.
- The real DDSM—what you learn in practice.
  Architecture and governing equations. What can go wrong and why?—telltale signs in the lab.
- Spurs and how to eliminate them.
  Identifying the sources of spurs and strategies to remove them. Stochastic techniques. Deterministic techniques. Hybrid techniques.
- Complexity reduction strategies facilitated by error-masking
  Error masking. Interstage quantization. Bus-splitting.

TUTORIALS

TUTORIAL 5

USING LOGICAL EFFORT FOR DESIGNING CARBON NANOTUBE FET (CNFET)-BASED DIGITAL CIRCUITS

Malgorzata Chrzanowska-Jeske
Electrical & Computer Engineering
Portland State University, USA

Sunday, December 9th, 2012 (15:00 - 19:00)
Room Andalucía 6

Abstract

Carbon Nanotube Field Effect Transistor (CNFET) is one of the most promising candidates for a building block of post silicon era integrated circuits because of its excellent electronic properties. Furthermore, am bipolar properties of carbon-nanotubes allow building compact generalized logic gates, based on XOR operations, and realizing many functions with fewer physical resources. CNT-based technology, however, is facing some major challenges; (1) variation in the diameter and density of the tubes that results in variation in delay and power consumption of CNT-based circuits, (2) the misalignment of CNTs that can result in incorrect logic functionality, (3) the presence of unwanted metallic carbon nanotubes, (4) the presence of Schottky barriers between the metal electrodes and the CNTs. This tutorial starts with a discussion on carbon nanotubes' electrical properties, possible CNFETs and simple gate configurations, and their performance, power and yield evaluation. A comparison with nano CMOS circuits will be presented as well. We will discuss technology challenges and current methods to dill with these challenges. One of the major challenges faced by the CNFET is the presence of unwanted metallic tubes that adversely impacts the delay, power and functional yield of CNT-based circuits. We will discuss CNFET-based circuit delay, power and yield in the presence variations of physical parameters of carbon nanotubes arrays, and variations due to removal of unwanted metallic tube. Monte Carlo simulations and results from newly developed analytical models are used to evaluate tradeoff between performance parameters and proposed gate- and circuit-level techniques to build robust circuits. Current technology, device, circuit and layout methods, to reduce impact of other challenges will be presented and future technology and research directions will be proposed and discussed. Logical Effort for basic CNFET logic gates will be derived, discussed, and used for performance and yield evaluation. We will present methods to evaluate

performance and yield of CNFET-based circuits in the presence of variations and the initial presence of metallic tubes. Comparison between CMOS and CNFET-based circuits will be presented using logical effort.

TUTORIAL 6

MEMRISTOR TECHNOLOGY IN NEUROMORPHIC CIRCUITS

Fernando Corinto
Department of Electronics and Telecommunications at Politecnico di Torino, Italy

Sunday, December 9th, 2012 (15:00 - 19:00)
Room Andalucía 7

Abstract
Conventional computing, including both hardware platforms and computer languages, seems to be close to its physical limits in terms of speed and data density. Classical Von Neumann architectures are known to be great in number crunching, nevertheless, they struggle with tasks like face recognition, real-time navigation control, object segmentation and depth perception. On top of that, CMOS technologies are also approaching the nano-scale floor, with devices attaining comparable dimensions to their constituting atoms, imposing significant challenges on the performance and reliability of analogue and digital circuits hindering the well-exploited correlation of Moore's law with computation capacity.
The imminent barriers to Moore's Law call for disruptive idea of VLSI building blocks for next generation electronics. Responsive efforts span from investigation of new physical state variables other than charge or voltage to novel nanoelectronic devices and circuit architectures offering ultra-dense memory, and low-power logic and reconfigurable hardware architectures. Memristors were first conjectured based on the missing constitutive link between flux and charge by Leon Chua as published in his seminal paper in 1971, which was further extended by L. O. Chua and S. M. Kang in their 1976 paper on memristive devices and systems. Recently physical realization of memristors was reported in Nature by HP's Stan Williams team in 2008. Memristor potential goes far beyond the attractive possibility of designing a computer where saving at shut down and rebooting at start up are unnecessary or a mobile phone where no battery charging is needed, including

TUTORIALS

one of the greatest technology challenges, i.e. mimicking the functionalities of the human brain. To date, memristor represents the latest technology breakthrough to build electronics devices with characteristics that show an intriguing resemblance to the brain's synapses.
The proposed tutorial aim to address a novel area of research that makes use of a disruptive technology as the fundamental bio-inspired computation element, the memristor.

Topics

- Neuromorphic circuits and Moore's Law
- Memristor and memristive devices: from theory to applications
- Memristor synapses for unconventional neuromorphic computing

TUTORIAL 7

LOW POWER DESIGN METHODOLOGY AND TECHNIQUES – INDUSTRIAL PERSPECTIVE

Kaijian Shi
Solution Architect
Cadence Design Systems, USA

Sunday, December 9th, 2012 (15:00 - 19:00)
Room Andalucía 8

Abstract
Power has become a critical metric and key differentiator in sub-65nm designs, due to growing power density driven by technology scaling and chip integration. This tutorial provides overview of the low- power design methodologies and techniques in production design perspective, emphasizing on the real design considerations and impact on chip success. We shall discuss pros and cons of the methods and techniques considering impacts on chip design schedule, yield, and overall power-performance target. We shall also provide design guidance and recommendations in various design steps and decision making points, based on our years of successful experience in production low-power SOC designs. This tutorial will start with overview of power related challenges in sub-60nm design and state-of-the-art power reduction techniques, and then detailed discussions about production low-power design methodology and techniques focusing on the power-gating and the voltage/frequency scaling which are the two advanced

power reduction methods used effectively in sub-65nm production low-power designs. We shall explain when, where and how these methods and techniques should be applied to a chip based on the design goals and time-to-market requirement. We shall also cover production low- power design methodology and flow with power intent and unified design environment.

The objective of this half-day tutorial is to addresses the needs in low-power design industry.

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

Analog Circuit Techniques I

Session Code: A1L-A (Lecture)

Location: Room Sevilla I

Date & Time: Monday, December 10th, 2012
(09:30 - 11:10)

Chair: Maurits Ortmanns
University of Ulm, Germany

09:30 **A Low Power Variable GBW Opamp from 60MHz to 2GHz for Multi-Standard Receivers**
A. Atac, C. Harder, R. Wunderlich, S. Heinen
RWTH Aachen University, Germany

09:50 **Low-Voltage CMOS Current Feedback Amplifier**
V. Pisani, I. Grech, O. Casha, E. Gatt
University of Malta, Malta

10:10 **Optimization Based on Surrogate Modeling for Analog Integrated Circuits**
F. Yengui, L. Labrak, P. Russo, F. Frantz, N. Abouchi
Lyon Institute of Nanotechnology, France

10:30 **Web-Based Analog Design Using Tradeoff Charts**
A. Hamza[1], A. Philip[1], M. Ali[1], M. Dessouky[2], M. Kassem[3]
[1] *Ain Shams University, Egypt*
[2] *Ain Shams University & Mentor Graphics Corp., Egypt*
[3] *Stone Soup Labs, USA*

10:50 **Ultra-Low Voltage Drain-Bulk Connected MOS Transistors in Weak and Moderate Inversion**
A. Dimakos[1], M. Bucher[1], R. Sharma[1], I. Chlis[2]
[1] *Technical University of Crete, Greece*
[2] *Columbia University, USA*

MONDAY, DECEMBER 10TH, 2012

Bioengineering Circuits and Systems I

Session Code: A1L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Monday, December 10th, 2012
(09:30 - 11:10)

Chair: Mohamad Sawan
École Polytechnique, University of Montreal, Canada

09:30 **Evaluating the Influence of the Bit Error Rate on the Information of Neural Spike Signals**
C. Bulach, U. Bihr, M. Ortmanns
Universität Ulm, Germany

09:50 **Towards an Optimized Wearable Neuromodulation Device for Urinary Incontinence**
A. Shiraz, A. Demosthenous, A. Vanhoestenberghe
University College London, UK

10:10 **Towards a Closed-Loop Transmitter System with Integrated Class-D Amplifier for Coupling-Insensitive Powering of Implants**
V. Valente, C. Eder, A. Demosthenous, N. Donaldson
University College London, UK

10:30 **Multi-Application Electrical Stimulator Architecture Dedicated to Waveform Control by Electrode-Tissue Impedance Spectra Monitoring**
F. Dupont, C. Condemine, J. Beche, M. Belleville
CEA-Leti, France

10:50 **Selection of Wavelet-Bands for Neural Network Discrimination of Parkinsonian Tremor from Essential Tremor**
A. Hossen
Sultan Qaboos University, Oman

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

Digital Signal Processing

Session Code: A1L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Monday, December 10th, 2012
(09:30 - 11:10)

Chair: Javier Castro
University of Seville, Spain

09:30 **Hardware-Efficient Matrix Inversion Algorithm for Complex Adaptive Systems**
A. Rosado[1], T. Iakymchuk[1], M. Bataller[1], M. Wegrzyn[2]
[1] *Universitat de València, Spain*
[2] *University of Zielona Góra, Poland*

09:50 **Implementation of a New Adaptive Algorithm Using Fuzzy Cost Function and Robust to Impulsive Noise**
T. Iakymchuk, A. Rosado, E. Soria-Olivas, M. Bataller
Universitat de València, Spain

10:10 **Rads Converter: an Approach to Analog to Information Conversion**
J. Haboba[1], R. Rovatti[1], G. Setti[2]
[1] *Università di Bologna, Italy*
[2] *Università degli Studi di Ferrara, Italy*

10:30 **High-Speed Compressed Sensing Reconstruction on FPGA Using OMP and AMP**
L. Bai, P. Maechler, M. Muehlberghuber, H. Kaeslin
ETH Zürich, Switzerland

MONDAY, DECEMBER 10TH, 2012

RF Building Blocks

Session Code: A1L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Monday, December 10th, 2012
(09:30 - 11:10)

Chair: Jorge Fernandes
Instituto Superior Técnico / INESC-ID, Portugal

09:30 **A Linearity Enhancement Technique and its Application to CMOS Wideband Low-Noise Amplifiers**
A. Masnadi Shirazi, H. Rashtian, S. Mirabbasi
University of British Columbia, Canada

09:50 **A 7GHz Wideband Self-Correcting Quadrature VCO**
T. Arai[1], A. Hajimiri[2]
[1] *Fujitsu Laboratories, USA*
[2] *California Institute of Technology, USA*

10:10 **Design Methodology and Integration of a 1.8GHz Outphasing Power Amplifier for Mobile Terminals**
O. Talebi Amiri, A. Koukab
École Polytechnique Fédérale de Lausanne, Switzerland

10:30 **4.0-5.5 GHz Tunable Power Splitter RFIC Using Active Inductors**
Y. Zheng, C. Saavedra
Queen's University, Canada

10:50 **Design of ADPLL System for WiMAX Applications in 40-nm CMOS**
W. Jiang[1], A. Tavakol[2], P. Effendrik[2], M. van de Gevel[3], F. Verwaal[3], R. Staszewski[2]
[1] *University of California, Los Angeles, USA*
[2] *Delft University of Technology, Netherlands*
[3] *Catena Microelectronics BV., Netherlands*

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

Computationally Intensive Applications on FPGAs

Session Code: A1L-E (Lecture) (Special Session)

Location: Room Andalucía 5

Date & Time: Monday, December 10th, 2012
(09:30 - 11:10)

Chair: Dionysios Reisis
National and Kapodistrian University of Athens, Greece

09:30 **A Soft IP Core Generating SoCs for the Efficient Stochastic Simulation of Large Biomolecular Networks Using FPGAs**
O. Hazapis, E. Logaras, E. Manolakos
University of Athens, Greece

09:50 **Signal Processing for Deep-Sea Observatories with Reconfigurable Hardware**
K. Manolopoulos[1], A. Belias[2], G. Georgis[1], D. Reisis[1], E. Anasontzis[1]
[1] *National and Kapodistrian University of Athens, Greece*
[2] *National Centre for Scientific Research-Demokritos, Greece*

10:10 **FPGA-Based Path-Planning of High Mobility Rover for Future Planetary Missions**
G. Lentaris[1], D. Diamantopoulos[1], J. Stamoulias[1], K. Siozios[1], D. Soudris[1], M. Avilés Rodrigálvarez[2]
[1] *National Technical University of Athens, Greece*
[2] *GMV, Spain*

10:30 **Hardware Design and Verification Techniques for Giga-bit Forward-Error Correction Systems on FPGAs**
A. Mahdi, P. Sakellariou, N. Kanistras, I. Tsatsaragkos, V. Paliouras
University of Patras, Greece

10:50 **FPGA Based Cellular Automata for Environmental Modeling**
I. Vourkas, G. Sirakoulis
Democritus University of Thrace, Greece

MONDAY, DECEMBER 10TH, 2012

Analog Circuit Techniques II

Session Code: A2L-A (Lecture)

Location: Room Sevilla I

Date & Time: Monday, December 10th, 2012
(11:30 - 13:10)

Chair: Maurits Ortmanns
University of Ulm, Germany

11:30 **A 6.66-kHz, 940-nW, 56PPM/°C, Fully on-Chip PVT Variation Tolerant CMOS Relaxation Oscillator**
K. Tsubaki, T. Hirose, Y. Osaki, S. Shiga, N. Kuroki, M. Numa
Kobe University, Japan

11:50 **Compact Class-AB Follower for Wideband Closed Loop Line Drivers**
D. Gascon, A. Sanuy, J. Sieiro
Universitat de Barcelona, Spain

12:10 **A Low-Distortion Switched-Source-Follower Track-and-Hold Circuit**
A. Moriyama, S. Taniyama, T. Waho
Sophia University, Japan

12:30 **A 2.5-GS/s 62dB THD SiGe Track-and-Hold Amplifier with Feedthrough Cancellation Technique**
D. Cascella, F. Cannone, G. Avitabile, G. Coviello
Politecnico di Bari, Italy

12:50 **A CMOS Track-and-Hold Circuit with Beyond 30 GHz Input Bandwidth**
B. Sedighi, A. Huynh, E. Skafidas
University of Melbourne, Australia

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

Sensing and Sensor Networks

Session Code: A2L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Monday, December 10th, 2012
(11:30 - 13:10)

Chair: Philippe Benabes
Supelec, France

11:30 **All-Digital A/D Converter TAD for Sensor Interface over Wide Temperature Ranges**
T. Watanabe, H. Isomura, T. Terasawa
DENSO Corporation, Japan

11:50 **A Readout Circuit Implementation to Reduce the Flicker Noise in MEMS Electrothermal Sensors**
A. Mohammadi[1], M. Yuce[2], R. Moheimani[1]
[1] *University of Newcastle, Australia*
[2] *Monash University, Australia*

12:10 **In Pixel Implementation of Autoadaptative Integration Time**
H. Abbass[1], H. Amhaz[1], G. Sicard[1], D. Alleysson[2]
[1] *TIMA Laboratory, France*
[2] *LPNC Laboratory, France*

12:30 **Design and Implementation of a Neurocomputing ASIP for Environmental Monitoring in WSN**
J. Rust, S. Paul
Universität Bremen, Germany

12:50 **A System-Proof-of-Concept for Remote Measurement Applications**
M. Mailand[1], S. Getzlaff[1], A. Dehennis[2]
[1] *Zentrum Mikroelektronik Dresden AG, Germany*
[2] *Senseonics, Incorporated, USA*

MONDAY, DECEMBER 10TH, 2012

DSP Algorithm and Implementation

Session Code: A2L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Monday, December 10th, 2012
(11:30 - 13:10)

Chairs: Antonio Acosta
Univ. of Seville & IMSE-CNM-CSIC, Spain
Javier Castro
University of Seville, Spain

11:30 **FPGA Implementation of Simple Digital Signal Processor**
M. Butorac, M. Vucic
University of Zagreb, Croatia

11:50 **Improving Palmprint Identification by Combining Multiple Classifiers and Using Gabor Filter**
A. Meraoumia[1], S. Chitroub[2], A. Bouridane[3]
[1] *Université Kasdi Merbah Ouargla, Algeria*
[2] *University of Sciences and Technology HOUARI BOUMEDIENE, Algeria*
[3] *Northumbria University & King Saudi University, Saudi Arabia*

12:10 **Protein Alignment HW/SW Optimizations**
G. Urgese, M. Graziano, M. Vacca, M. Awais, S. Frache, M. Zamboni
Politecnico di Torino, Italy

12:30 **Parallel Scaling-Free and Area-Time Efficient CORDIC Algorithm**
M. Causo, T. An, L. Alves de Barros Naviner
Institut Mines-Telecom, Télécom ParisTech, France

12:50 **A VLSI Architecture for Multiple Antenna Eigenvalue-Based Spectrum Sensing**
S. Safavi, M. Shabany
Sharif University of Technology, Iran

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

RF and mmWave Circuits

Session Code: A2L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Monday, December 10th, 2012
(11:30 - 13:10)

Chair: Jorge Fernandes
Instituto Superior Técnico / INESC-ID, Portugal

11:30 **A 1-mW Current Reuse Quadrature RF Front-End for GPS L1 Band in 0.18µm CMOS**
H. Jalili[1], A. Fotowat-Ahmady[1], M. Jenabi[2]
[1] *Sharif University of Technology, Iran*
[2] *Unistar Micro Technology Inc., Canada*

11:50 **A Power-Scalable RF CMOS Receiver for 2.4 GHz Wireless Sensor Network Applications**
K. Ghosal, T. Anand, V. Chaturvedi, B. Amrutur
Indian Institute of Science, India

12:10 **A 20 Mb/s 0.084 nJ/bit ISM-Band Transmitter Dedicated to Medical Sensor Networks**
A. Moradi, M. Sawan
École Polytechnique de Montréal, Canada

12:30 **Analysis and Characterization of Mismatches in Outphasing Transmitter**
S. Kulkarni, D. Zhao, P. Reynaert
Katholieke Universiteit Leuven, Belgium

12:50 **A 60GHz Class F-E Power VCO with Vector-Modulator Feedback in 65nm CMOS Technology**
S. Dréan[1], N. Martin[2], N. Deltimple[2], E. Kerhervé[2], B. Martineau[1], D. Belot[1]
[1] *STMicroelectronics, France*
[2] *IMS Laboratory, France*

MONDAY, DECEMBER 10TH, 2012

Analog Circuit Techniques III

Session Code: A3L-A (Lecture)

Location: Room Sevilla I

Date & Time: Monday, December 10th, 2012
(14:40 - 16:20)

Chair: Maurits Ortmanns
University of Ulm, Germany

14:40 **A Low-Power CMOS RF Power Detector**
S. Sakphrom, A. Thanachayanont
King Mongkut's Institute of Technology Ladkrabang, Thailand

15:00 **Millimeter-Wave High-Q Active Inductor in 65nm CMOS**
D. Pepe[1], D. Zito[1,2]
[1] *Tyndall National Institute, Ireland*
[2] *University College Cork, Ireland*

15:20 **Windowed Phase Comparator for an 80Gbit/s CDR**
Q. Béraud-Sudreau[1], O. Mazouffre[1], M. Pignol[2], L. Baguena[3], C. Neveu[3], J. Begueret[1], T. Taris[1]
[1] *L'Université de Bordeaux, France*
[2] *CNES, France*
[3] *Thales Alenia Space, France*

15:40 **A Novel Multi-Step C-2C DAC Architecture**
M. Abedinkhan[1], A. Sodagar[1], R. Mohammadi[1], P. Adl[2]
[1] *K. N. Toosi University of Technology, Iran*
[2] *Brunel University, UK*

16:00 **A CMOS 0.13µm Low Power Front-End for GEM Detectors**
A. Costantini[1], A. Pezzotta[1], A. Baschirotto[1], M. De Matteis[1], S. D'Amico[2], F. Murtas[3], G. Gorini[1]
[1] *Università degli Studi di Milano-Bicocca, Italy*
[2] *Università del Salento, Italy*
[3] *INFN-Frascati, Italy*

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

Sensors and Photonics

Session Code: A3L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Monday, December 10th, 2012
(14:40 - 16:20)

Chair: Henry Radamson
KTH Royal Institute of Technology, Sweden

14:40 **All-Digital A/D Converter TAD for High-Resolution and Low-Power Sensor/RF Interface**
T. Watanabe, T. Terasawa
DENSO Corporation, Japan

15:00 **Temperature Considerations on Hall Effect Sensors Current-Related Sensitivity Behaviour**
M. Paun, J. Sallese, M. Kayal
École Polytechnique Fédérale de Lausanne, Switzerland

15:20 **A Tri-Mode Event-Based Vision Sensor with an Embedded Wireless Transmitter**
J. Leñero-Bardallo[1], W. Tang[2], D. Kim[3], J. Park[2], E. Culurciello[4]
[1] *Universitetet i Oslo, Norway*
[2] *Yale University, USA*
[3] *Aptina Imaging, USA*
[4] *Purdue University, USA*

15:40 **Improved High Precision Optical Angle Measurement System with No Interference of Light Gradients and Mismatch**
J. Oehm, C. Koch, I. Stoychev, A. Gornik
Ruhr Universitaet, Germany

16:00 **A 10Gb/s Inductorless Push Pull Current Mirror Transimpedance Amplifier**
M. Hassan, H. Zimmermann
Technische Universität Wien, Austria

MONDAY, DECEMBER 10TH, 2012

Digital Circuits on FPGAs

Session Code: A3L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Monday, December 10th, 2012
(14:40 - 16:20)

Chair: Antonio Acosta
Univ. of Seville & IMSE-CNM-CSIC, Spain

14:40 **Performance Evaluation for FPGA-Based Processing of Tree-Like Structures**
V. Sklyarov[1], I. Skliarova[1], D. Mihhailov[2], A. Sudnitson[2]
[1] *Universidade de Aveiro, Portugal*
[2] *Tallinn University of Technology, Estonia*

15:00 **FPGA Implementation of Very High Radix Square Root with Prescaling**
A. Amaricai, O. Boncalo
University Politehnica of Timisoara, Romania

15:20 **Performance Evaluation of RAM-Based Implementation of Finite State Machines in FPGAs**
R. Senhadji-Navarro, I. García-Vargas, J. Guisado
Universidad de Sevilla, Spain

15:40 **FPGA-Based Autonomous Parking of a Car-Like Robot Using Fuzzy Logic Control**
N. Scicluna, E. Gatt, O. Casha, I. Grech, J. Micallef
University of Malta, Malta

16:00 **A Generic FPGA Emulation Framework**
F. Moraes, M. Moreira, C. Lucas, D. Corrêa, D. Cardoso, M. Magnaguagno, G. Castilhos, N. Calazans
Pontifícia Universidade do Rio Grande do Sul, Brazil

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

Wireless and Wireline Communications

Session Code: A3L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Monday, December 10th, 2012
(14:40 - 16:20)

Chair: Jorge Fernandes
Instituto Superior Técnico / INESC-ID, Portugal

14:40 **Design of a 80 Gbit/s SiGe BiCMOS Fully Differential Input Buffer for Serial Electrical Communication**
T. De Keulenaer, Y. Ban, Z. Li, J. Bauwelinck
Ghent University, Belgium

15:00 **A Power Efficient 3-Gbits/s 1.8V PMOS-Based LVDS Output Driver**
H. Marar[1], K. Abugharbieh[1], A. Al-Tamimi[2]
[1] *Princess Sumaya University for Technology, Jordan*
[2] *Yarmouk University, Jordan*

15:20 **Accessible Approach to Wideband Matching**
A. Lehtovuori, R. Valkonen, M. Valtonen
Aalto University, Finland

15:40 **A Generalized Graphical Model to Specify A/D Resolution from Receiver Front-End**
S. Wang, C. Dehollain
École Polytechnique Fédérale de Lausanne, Switzerland

MONDAY, DECEMBER 10TH, 2012

Analog Filters

Session Code: A4L-A (Lecture)

Location: Room Sevilla I

Date & Time: Monday, December 10th, 2012 (17:10 - 18:50)

Chair: Maurits Ortmanns
University of Ulm, Germany

17:10 **Lumped-Element-Based Single/Dual-Passband Analog Filters Using Signal-Interference Principles**
R. Loeches-Sánchez[1], R. Gómez-García[1], B. Jarry[2], J. Lintignat[2], B. Barelaud[2]
[1] *Universidad de Alcalá, Spain*
[2] *Université de Limoges, France*

17:30 **Self-Biased Input Common-Mode Generation for Improving Dynamic Range and Yield in Inverter-Based Filters**
A. Ginés, A. Villegas, E. Peralías, A. Rueda
Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain

17:50 **A 1.25mW 3rd-Order Active-Gm-RC 250MHz-Bandwidth Analog Filter Based on Power-Stability Optimization**
M. De Matteis[1], S. D'Amico[2], A. Costantini[1], A. Baschirotto[1]
[1] *Università degli Studi di Milano-Bicocca, Italy*
[2] *Università del Salento, Italy*

18:10 **Dynamic Range Improvement of New Leap-Frog Filter Using Numerical Optimization**
D. Jurisic[1], N. Mijat[1], G. Moschytz[2]
[1] *University of Zagreb, Croatia*
[2] *Bar-Ilan University, Israel*

18:30 **A Fourth Order CMOS Band Pass Filter for PIR Sensors**
G. Doménech-Asensi[1], F. Martínez-Viviente[1], J. Illade-Quinteiro[1], J. Zapata-Pérez[1], R. Ruiz-Merino[1], J. López-Alcantud[1], J. Martínez-Alajarín[1], F. Fernández-Luque[1], J. Carrillo[2], M. Domínguez[2]
[1] *Universidad Politécnica de Cartagena, Spain*
[2] *Universidad de Extermadura, Spain*

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

Mixed-Signal Test and Verification

Session Code: A4L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Monday, December 10th, 2012
(17:10 - 18:50)

Chairs: Diego Vázquez
Univ. of Seville & IMSE-CNM-CSIC, Spain
Salvador Mir
TIMA, France

17:10 **Accurate Estimation of Analog Test Metrics with Extreme Circuits**
K. Beznia[1], A. Bounceur[1], L. Abdallah[2], K. Huang[2], S. Mir[2], R. Euler[1]
[1] *Université de Bretagne Occidentale, France*
[2] *TIMA Laboratory, France*

17:30 **Single Pass Temperature Calibration of the ASIC on a General Purpose ATE**
J. Trontelj Jr., B. Šmid, J. Trontelj
University of Ljubljana, Slovenia

17:50 **A Template for the Construction of Efficient Checkers with Full Verification Guarantees**
L. Freitas, G. Andrade, L. Dos Santos
Universidade Federal de Santa Catarina, Brazil

18:10 **A Formal Framework for Testing with Assertion Checkers in Mixed-Signal Simulation**
L. Pierre
TIMA Laboratory, France

MONDAY, DECEMBER 10TH, 2012

VLSI Digital Implementations

Session Code: A4L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Monday, December 10th, 2012
(17:10 - 18:50)

Chair: Antonio Acosta
Univ. of Seville & IMSE-CNM-CSIC, Spain

17:10 **Design and Characterization of a QLUT in a Standard CMOS Process**
D. Brito, J. Fernandes, P. Flores, J. Monteiro
INESC-ID / IST / Universidade Técnica de Lisboa, Portugal

17:30 **Dual-Edge Triggered Sense Amplifier Flip-Flop Utilizing an Improved Scheme to Reduce Area, Power, and Complexity**
S. Esmaeili[1], R. Islam[2], A. Al-Khalili[1], G. Cowan[1]
[1] *Concordia University, Canada*
[2] *École Polytechnique de Montréal, Canada*

17:50 **Maximum Delay Variation Temperature-Aware Standard Cell Design**
M. Pons, J. Nagel, C. Piguet
CSEM S.A, Switzerland

18:10 **A Low Complexity Architecture for the Cell Search Applied to the LTE Systems**
A. Golnari[1], G. Sharifan[2], Y. Amini[2], M. Shabany[3]
[1] *Princeton University, USA*
[2] *Sharif University of Technology, Iran*
[3] *University of Toronto, Canada*

18:30 **Digitizing the Yuan Tseh Lee Array for Microwave Background Anisotropy by 5Gsps ADC Boards**
H. Jiang, H. Liu, K. Guzzino, D. Kubo, C. Li, R. Chang
Institute of Astronomy and Astrophysics, Academia Sinica, Taiwan

LECTURE SESSIONS

MONDAY, DECEMBER 10TH, 2012

Algorithms for Communications

Session Code: A4L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Monday, December 10th, 2012
(17:10 - 18:50)

Chair: Thanos Stouraitis
University of Patras, Greece

17:10 **PMEPR Reduction for OFCDM Using SLM and PTS**
M. Syed, A. Umrani, A. Memon, M. Syed
Mehran University of Engineering & Technology, Pakistan

17:30 **Adaptive Slope and Threshold Companding Technique for PAPR Reduction in OFDM Systems**
V. Yenamandra[1], F. Lei[1], S. Al-Araji[2], N. Ali[2], M. Ismail[3]
[1] *Ohio State University, USA*
[2] *Khalifa University, U.A.E.*
[3] *Khalifa University of Science Technology & Research, U.A.E.*

17:50 **Selective Channelization on an SDR Platform for LTE-A Carrier Aggregation**
I. Diaz[1], R. Torrea-Duran[2], S. Pollin[2], L. Van der Perre[2], V. Öwall[1]
[1] *Lund University, Sweden*
[2] *IMEC, Belgium*

18:10 **A Novel Implementation of Sequential Output Based Parallel Processing - Orthogonal Wavelet Division Multiplexing for Das on SDR Platform**
C. Mahapatra[1], A. Ramakrishnan[1], T. Stouraitis[2], V. Leung[1]
[1] *University of British Columbia, Canada*
[2] *University of Patras, Greece*

MONDAY, DECEMBER 10TH, 2012

Advances in Embedded Vision Hardware

Session Code: A4L-E (Lecture) (Special Session)

Location: Room Andalucía 5

Date & Time: Monday, December 10th, 2012
(17:10 - 18:50)

Chair: Jorge Fernández-Berni
University of Seville, Spain

17:10 **Mixed Signal SIMD Cellular Processor Array Vision Chip Operating at 30,000 fps**
S. Carey, D. Barr, B. Wang, A. Lopich, P. Dudek
University of Manchester, UK

17:30 **Bottom-Up Visual Attention Model Based on FPGA**
F. Barranco, J. Diaz, B. Pino, E. Ros
Universidad de Granada, Spain

17:50 **CMOS SPADs Selection, Modeling and Characterization Towards Image Sensors Implementation**
M. Moreno García, O. Guerra Vinuesa, R. del Río Fernández, B. Pérez Verdú, Á. Rodríguez Vázquez
Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain

18:10 **Embedded Low-Power Low-Cost Camera Sensor Based on FPGA and its Applications in Mobile Robots**
J. Albo-Canals, S. Ortega, S. Perdices, A. Badalov, X. Vilasis-Cardona
Universitat Ramon Llull, Spain

18:30 **High Dynamic Range Image Sensor with Self Adapting Integration Time in 3D Technology**
F. Guezzi-Messaoud[1], A. Dupret[1], A. Peizerat[1], Y. Blanchard[2]
[1] *CEA LETI DACLE L3I, France*
[2] *ESIEE PARIS, France*

LECTURE SESSIONS

TUESDAY, DECEMBER 11TH, 2012

Data Converters

Session Code: B1L-A (Lecture)

Location: Room Sevilla I

Date & Time: Tuesday, December 11th, 2012
(09:30 - 11:10)

Chair: Saul Rodriguez
Royal Institute of Technology (KTH), Sweden

09:30 **A/D Conversion of the Battery Voltage in Advanced CMOS Technologies**
M. Zamprogno, A. Minuti, F. Girardi, G. Nicollini
ST-Ericsson, Italy

09:50 **On the Design of a 2-2-0 MASH Delta-Sigma-Pipeline Modulator**
R. Mohammadi, H. Shamsi, M. Abedinkhan
K. N. Toosi University of Technology, Iran

10:10 **Analysis of VCO Based Noise Shaping ADCs Linearized by PWM Modulation**
L. Hernandez[1], E. Prefasi[1], S. Paton[1], P. Rombouts[2]
[1] *Universidad Carlos III de Madrid, Spain*
[2] *Universiteit Gent, Belgium*

10:30 **Design of an Undersampled BP Sigma-Delta Modulator Using LC and Time-Interleaved Resonators**
N. Beilleau[1], V. Bourguet[1], F. Rangel de Sousa[2]
[1] *Universidade Federal do Rio Grande do Norte, Brazil*
[2] *Universidade Federal de Santa Catarina, Brazil*

10:50 **Incremental-Sigma-Delta-ADCs with Dynamic Conversion Length Adaption**
J. Uhlig, R. Schüffny
Technische Universität Dresden, Germany

TUESDAY, DECEMBER 11TH, 2012

Bioengineering Circuits and Systems II

Session Code: B1L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Tuesday, December 11th, 2012
(09:30 - 11:10)

Chair: Manuel Delgado-Restituto
IMSE-CNM-CSIC, Spain

09:30 **Interpolation Filter Design for Hearing-Aid Audio Class-D Output Stage Application**
P. Pracný, P. Llimós Muntal, E. Bruun
Danmarks Tekniske Universitet, Denmark

09:50 **Dual Data Pulse Width Modulator for Wireless Simultaneous Measurement of Redox Potential and Temperature Using a Single RFID Chip**
B. Kim, K. Nakazato
Nagoya University, Japan

10:10 **The Wireless System for Egg Signal Acquisition**
D. Komorowski, S. Pietraszek, D. Grzechca
Silesian University of Technology, Poland

10:30 **A High Dynamic Range Wideband CMOS Phase Angle Detector for Bioimpedance Spectroscopy**
J. Ausín[1], J. Ramos[1], F. Duque-Carrillo[1], G. Torelli[2]
[1] *Universidad de Extremadura, Spain*
[2] *Università degli studi di Pavia, Italy*

LECTURE SESSIONS

TUESDAY, DECEMBER 11TH, 2012

Digital Circuits for Embedded Control and Security

Session Code: B1L-C (Lecture) (Special Session)

Location: Room Andalucía 7

Date & Time: Tuesday, December 11th, 2012 (09:30 - 11:10)

Chair: Marco Storace
Unversity of Genova, Italy

09:30 **Hardware-in-the-Loop Simulations of Circuit Architectures for the Computation of Exact and Approximate Explicit MPC Control Functions**
A. Oliveri, M. Storace
DITEN, University of Genoa, Italy

09:50 **VLSI Implementation of Digital Frequency Sensors as Hardware Countermeasure**
R. Jiménez, G. Feria, J. Gómez Galán, F. Gómez-Bravo, M. Sánchez
Universidad de Huelva, Spain

10:10 **ASIC-in-the-Loop Methodology for Verification of Piecewise Affine Controllers**
M. Martínez-Rodríguez, P. Brox, J. Castro, E. Tena, A. Acosta, I. Baturone
Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain

10:30 **Reducing Bit Flipping Problems in SRAM Physical Unclonable Functions for Chip Identification**
S. Eiroa, J. Castro, M. Martínez-Rodríguez, E. Tena, P. Brox, I. Baturone
Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain

TUESDAY, DECEMBER 11TH, 2012

Digital Circuits for Channel Coding

Session Code: B1L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Tuesday, December 11th, 2012
(09:30 - 11:10)

Chair: Piedad Brox
IMSE-CNM-CSIC, Spain

09:30 **Low Energy High Speed Reed-Solomon Decoder Using Two Parallel Modified Evaluator Inversionless Berlekamp-Massey**
H. Ahmed[1], H. Salah[1], T. Elshabrawy[1], H. Fahmy[2]
[1] *German University in Cairo, Egypt*
[2] *Cairo University, Egypt*

09:50 **High Speed Low Complexity Radix-16 Max-Log-MAP SISO Decoder**
O. Sánchez[1], C. Jégo[2], M. Jézéquel[1], Y. Saouter[1]
[1] *Institut Mines-Télécom/Télécom-Bretagne, France*
[2] *Université de Bordeaux, France*

10:10 **High-Throughput FPGA-Based Emulator for Structured LDPC Codes**
F. Angarita, V. Torres, A. Pérez-Pascual, J. Valls
Universidad Politecnica de Valencia, Spain

10:30 **Fully-Parallel LUT-Based (2048,1723) LDPC Code Decoder for FPGA**
V. Torres, A. Perez-Pascual, T. Sansaloni, J. Valls
Universidad Politecnica de Valencia, Spain

10:50 **Decoder for an Enhanced Serial Generalized Bit Flipping Algorithm**
F. García-Herrero, M. Canet, J. Valls
Universidad Politecnica de Valencia, Spain

LECTURE SESSIONS

TUESDAY, DECEMBER 11TH, 2012

Oversampling Data Converters

Session Code: B2L-A (Lecture)

Location: Room Sevilla I

Date & Time: Tuesday, December 11th, 2012
(11:30 - 13:10)

Chair: Saul Rodriguez
Royal Institute of Technology (KTH), Sweden

11:30 **Dynamic Range Improvement in 2nd-Order Low-Pass Multibit Sigma-Delta Modulators**
A. Barbieri, S. Pernici, G. Nicollini
ST-Ericsson, Italy

11:50 **Performance Tuning of Multi-Bit Continuous Time Sigma-Delta Modulators Using a Switched System Model**
C. Zorn[1], T. Brückner[2], M. Ortmanns[2], W. Mathis[1]
[1] *Leibniz Universität Hannover, Germany*
[2] *Universität Ulm, Germany*

12:10 **Analysis of Exponentially Decaying Pulse Shape DACs in Continuous-Time Sigma-Delta Modulators**
S. Tao, J. Garcia, S. Rodriguez, A. Rusu
KTH Royal Institute of Technology, Sweden

12:30 **Joint Estimation of Filter Nonidealities in Continuous-Time Sigma-Delta Modulators by Using an Unscented Kalman Filter**
M. Lorenz[1], M. Maurer[2], Y. Manoli[2], M. Ortmanns[1]
[1] *Universität Ulm, Germany*
[2] *German Albert-Ludwigs-Universität Freiburg / IMTEK, Germany*

12:50 **Discrete-Time Simulation of Arbitrary Digital/ Analog Converter Waveforms in Continuous-Time Sigma-Delta Modulators**
T. Brückner[1], M. Kiebler[1], C. Zorn[2], W. Mathis[2], M. Ortmanns[1]
[1] *Universität Ulm, Germany*
[2] *Leibniz Universität Hannover, Germany*

TUESDAY, DECEMBER 11TH, 2012

Analysis and Design Techniques for Low-Power Circuits

Session Code: B2L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Tuesday, December 11th, 2012 (11:30 - 13:10)

Chair: Vojin G. Oklobdzija
University of California. ACSEL Laboratory, USA

11:30 **CBSC-Based Pipelined Analog-to-Digital Converters: Power Dissipation Bound Analysis**
M. Zamani, C. Eder, A. Demosthenous
University College London, UK

11:50 **Peak Power Estimation Using Activity Measured on Emulator**
C. Berthet, P. Georgelin, J. Ntyame, M. Raffin
STMicroelectronics, France

12:10 **A Dual Threshold Voltage Technique for Glitch Minimization**
M. Slimani[1], P. Matherat[2], Y. Mathieu[1]
[1] *Institut TELECOM, TELECOM-ParisTech, LTCI-CNRS, France*
[2] *Institut Mines-Telecom, Télécom ParisTech, France*

12:30 **A 100-fJ/Cycle Sub-VT Decimation Filter Chain in 65 nm CMOS**
S. Sherazi, P. Nilsson, H. Sjöland, J. Rodrigues
Lund University, Sweden

12:50 **Low-Power Two's-Complement Multiplication Based on Selective Activation**
P. Sakellariou, V. Paliouras
University of Patras, Greece

LECTURE SESSIONS

TUESDAY, DECEMBER 11TH, 2012

Circuit Level CAD

Session Code: B2L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Tuesday, December 11th, 2012
(11:30 - 13:10)

Chair: Ricardo Reis
Universidade Federal do Rio Grande do Sul, Brazil

11:30 **Efficient Optimization Methodology for CT Functions Based on a Modified Bayesian Kriging Approach**
C. Tugui, R. Benassi, S. Apostol, P. Benabes
Supelec, France

11:50 **An Efficient Solution Space for Floorplan of 3D-LSI**
H. Tezuka, K. Fujiyoshi
Tokyo University of Agriculture and Technology, Japan

12:10 **Fast Floorplanning for Fixed-Outline and Non-Rectangular Regions**
M. Ahmed, S. Pinge, M. Chrzanowska-Jeske
Portland State University, USA

12:30 **Lagrangian Relaxation-Based Discrete Gate Sizing for Leakage Power Minimization**
V. Dos S. Livramento[1], C. Guth[1], J. Güntzel[1], M. Johann[2]
[1] *Universidade Federal de Santa Catarina, Brazil*
[2] *Universidade Federal do Rio Grande do Sul, Brazil*

12:50 **Finding the Hamiltonian Circuits in an Undirected Graph Using the Mesh-Links Incidence**
C. Onete[1], M. Onete[2]
[1] *NXP Semiconductors, Netherlands*
[2] *CASED & Technische Universität Darmstadt, Germany*

TUESDAY, DECEMBER 11TH, 2012

Nonlinear Circuits and Systems I

Session Code: B2L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Tuesday, December 11th, 2012 (11:30 - 13:10)

Chair: Sergio Callegari
Università di Bologna, Italy

11:30 **Improved Linearization of a High Power Amplifier to Reduce Spectral Distortions near the Saturation Area**
M. Brandon[1,2], M. Ariaudo[2], S. Traverso[1], J. Bouvier[1], J. Gautier[2], I. Fijalkow[2]
[1] *THALES Communications and Security, France*
[2] *Université de Cergy-Pontoise, France*

11:50 **Bifurcation Diagrams in MOS-NDR Frequency Divider Circuits**
J. Núñez, M. Avedillo, J. Quintana
Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain

12:10 **Nonlinear Harmonic Analysis of Multistage Amplifiers**
A. Buonomo, A. Lo Schiavo
Seconda Università degli Studi di Napoli, Italy

12:30 **A "Divide-by-Odd Number" Direct Injection CMOS LC Injection-Locked Frequency Divider**
M. Awan[1], M. Asghar[1], M. Kennedy[2]
[1] *Linkoping University, Sweden*
[2] *University College Cork, Ireland*

12:50 **Design for Linearizability of GaN Based Multi-Carrier Doherty Power Amplifier Through Bias Optimization**
O. Hammi[1], S. Jung[2], F. Ghannouchi[2]
[1] *King Fahd University of Petroleum and Minerals, Saudi Arabia*
[2] *University of Calgary, Canada*

LECTURE SESSIONS

TUESDAY, DECEMBER 11TH, 2012

Nyquist Rate Data Converters

Session Code: B3L-A (Lecture)

Location: Room Sevilla I

Date & Time: Tuesday, December 11th, 2012
(14:40 - 16:20)

Chair: Eduard Alarcón
Technical University of Catalunya (UPC), Spain

14:40 **A 4-bit 1.5GSps 4.2mW Comparator-Based Binary Search ADC in 90nm**
T. Rabuske[1], F. Rabuske[2], J. Fernandes[3], C. Rodrigues[2]
[1] *INESC-ID / Instituto Superior Técnico, Portugal*
[2] *Universidade Federal de Santa Maria, Brazil*
[3] *INESC-ID / IST / Universidade Técnica de Lisboa, Portugal*

15:00 **A 749nW 1MSps 8-bit SAR ADC at 0.5V Employing Boosted Switches**
T. Rabuske[1], J. Fernandes[2], S. Nooshabadi[3], C. Rodrigues[4], F. Rabuske[4]
[1] *INESC-ID / Instituto Superior Técnico, Portugal*
[2] *INESC-ID / IST / Universidade Técnica de Lisboa, Portugal*
[3] *Michigan Technological University, USA*
[4] *Universidade Federal de Santa Maria, Brazil*

15:20 **A Low-Power Fully Differential Cyclic 9-bit ADC**
N. Bako, A. Baric
University of Zagreb, Croatia

15:40 **Design of Hybrid Resistive-Capacitive DAC for SAR A/D Converters**
B. Sedighi[1], A. Huynh[1], E. Skafidas[1], D. Micusik[2]
[1] *University of Melbourne, Australia*
[2] *IHP Microelectronics, Germany*

16:00 **A 11B 5.1µW Multi-Slope ADC with a TDC Using Multi-Phase Clock Signals**
K. Kim, M. Ikebe, J. Motohisa, E. Sano
Hokkaido University, Japan

Circuit Techniques for Energy Harvesting Applications

Session Code: B3L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Tuesday, December 11th, 2012 (14:40 - 16:20)

Chair: Shahriar Mirabbasi
University of British Columbia, Canada

14:40 **An Ultra-Low Power Li-Ion Battery Charger for Micro-Power Solar Energy Harvesting Applications**
N. Khosro Pour, S. Facchin, F. Krummenacher, M. Kayal
École Polytechnique Fédérale de Lausanne, Switzerland

15:00 **A Passive CMOS Rectifier with Leakage Current Control for Medical Implants**
M. Ghanad, C. Dehollain
École Polytechnique Fédérale de Lausanne, Switzerland

15:20 **Design Comparison of Low-Power Rectifiers Dedicated to RF Energy Harvesting**
D. Karolak[1], T. Taris[1], Y. Deval[1], J. Béguéret[1], A. Mariano[2]
[1] *L'Université de Bordeaux, France*
[2] *Universidade Federal do Paraná, Brazil*

15:40 **A Process-Compatible Passive RFID Tag's Digital Design for Subthreshold Operation**
W. Shi[1], C. Choy[2]
[1] *Shenzhen University, China*
[2] *Chinese University of Hong Kong, Hong Kong*

16:00 **Design and Analysis of Multi-Core Homogeneous Systems for Energy Harvesting Applications**
M. Srivastav, L. Nazhandali
Virginia Polytechnic Institute and State University, USA

LECTURE SESSIONS

TUESDAY, DECEMBER 11TH, 2012

Methodologies for Systems-on-Chip

Session Code: B3L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Tuesday, December 11th, 2012
(14:40 - 16:20)

Chair: Kaijian Shi
Cadence Design Systems, USA

14:40 **On AOP Techniques for C++-Based HW/SW Component Implementation**
T. Mück, A. Fröhlich
Universidade Federal de Santa Catarina, Brazil

15:00 **An RTL Method for Hiding Clock Domain Crossing Latency**
G. Tarawneh, A. Yakovlev
Newcastle University, UK

15:20 **Enhancing Performance of MPSoCs Through Distributed Resource Management**
M. Mandelli, G. Castilhos, F. Moraes
Pontifícia Universidade do Rio Grande do Sul, Brazil

15:40 **Evaluation of Adaptive Management Techniques in NoC-Based MPSoCs**
F. Moraes[1], E. Carara[2], M. Ruaro[1], G. Madalozzo[1]
[1] *Pontifícia Universidade do Rio Grande do Sul, Brazil*
[2] *Universidade Federal de Santa Maria, Brazil*

16:00 **A Redundant Wire Addition Method for Patchable Accelerator**
M. Wakizaka[1], H. Yoshida[2], Y. Hara-Azumi[3], S. Yamashita[1]
[1] *Ritsumeikan University, Japan*
[2] *Fujitsu Laboratories of America, Inc, Japan*
[3] *Nara Institute of Science and Technology, Japan*

TUESDAY, DECEMBER 11TH, 2012

Multimedia Systems and Signal Processing I

Session Code: B3L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Tuesday, December 11th, 2012
(14:40 - 16:20)

Chair: Sergio Bampi
Universidade Federal do Rio Grande do Sul, Brazil

14:40 **Hybrid Multiple Constant Multiplication for FPGAs**
M. Kumm, P. Zipf
Universität Kassel, Germany

15:00 **Scene-Based Noise Reduction on a Smart Camera**
F. Hamdi, T. Toczek, B. Heyrman, D. Ginhac
Université de Bourgogne, France

15:20 **Dynamic Tree-Depth Adjustment for Low Power HEVC Encoders**
G. Correa[1], P. Assuncao[2], L. da Silva Cruz[1], L. Agostini[3]
[1] *Universidade de Coimbra / Instituto de Telecomunicações, Portugal*
[2] *Polytechnic Institute of Leiria, Portugal*
[3] *Universidade Federal de Pelotas, Brazil*

15:40 **Fast HEVC Intra Mode Decision Based on Dominant Edge Evaluation and Tree Structure Dependencies**
T. da Silva[1], L. da Silva Cruz[2], L. Agostini[3]
[1] *University of Coimbra, Portugal*
[2] *Universidade de Coimbra / Instituto de Telecomunicações, Portugal*
[3] *Universidade Federal de Pelotas, Brazil*

16:00 **A High Quality Hardware Friendly Motion Estimation Algorithm Focusing in HD Videos**
P. Dall'Oglio, C. Cristani, M. Porto, L. Agostini
Universidade Federal de Pelotas, Brazil

LECTURE SESSIONS

WEDNESDAY, DECEMBER 12TH, 2012

RF Circuits and Techniques I

Session Code: C1L-A (Lecture)

Location: Room Sevilla I

Date & Time: Wednesday, December 12th, 2012
(09:30 - 11:10)

Chair: Eduard Alarcón
Technical University of Catalunya (UPC), Spain

09:30 **Multiband Integrated Synthetic Aperture Radar (SAR) Receiver**
F. Abu Bakar[1], J. Holmberg[2], T. Nieminen[1], Q. Nehal[1], P. Ukkonen[1], V. Saari[1], K. Halonen[1], M. Aberg[2], I. Sundberg[3]
[1] *Aalto University, Finland*
[2] *VTT Technical Research Centre of Finland, Finland*
[3] *DA-Design Oy, Finland*

09:50 **Low-Power Area-Efficient Delay Element with a Wide Delay Range**
J. Al-Eryani[1], A. Stanitzki[2], K. Konrad[3], N. Tavangaran[3], D. Brückmann[3], R. Kokozinski[1]
[1] *Universität Duisburg-Essen, Germany*
[2] *Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme, Germany*
[3] *Universität Wuppertal, Germany*

10:10 **Skin Effect Modeling in Time Domain for RF Network on Chip**
L. Zerioul[1], E. Bourdel[1], M. Ariaudo[2]
[1] *ETIS Lab, France*
[2] *Université de Cergy-Pontoise, France*

10:30 **Stochastic Differential Equations Approach in the Analysis of MTLs with Randomly Varied Parameters**
L. Brancík, E. Kolárová
Brno University of Technology, Czech Rep.

10:50 **A RF/DC Current-Mode Detector for BiST and Digital Calibration of Current-Driven Mixers**
F. Lei[1], V. Yenamandra[1], S. Bibyk[1], M. Ismail[2]
[1] *Ohio State University, USA*
[2] *Khalifa University of Science Technology & Research, U.A.E.*

WEDNESDAY, DECEMBER 12TH, 2012

Emerging Technologies I

Session Code: C1L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Wednesday, December 12th, 2012 (09:30 - 11:10)

Chair: Fernando Corinto
Politecnico di Torino, Italy

09:30 **A Dual-Axis Bulk Micromachined Accelerometer with Low Cross-Sensitivity**
A. Alfaifi[1], F. Nabki[2], M. El-Gamal[1]
[1] *McGill University, Canada*
[2] *Université du Québec à Montréal, Canada*

09:50 **TSV Stress-Aware Performance and Reliability Analysis**
M. Ali, M. Ahmed, M. Chrzanowska-Jeske
Portland State University, USA

10:10 **FFT Implementation Using QCA**
M. Awais, M. Vacca, M. Graziano, G. Masera
Politecnico di Torino, Italy

10:30 **Analysis of Coupling Capacitance Between TSVs and Metal Interconnects in 3D-ICs**
K. Salah
Mentor Graphics, Egypt

LECTURE SESSIONS

WEDNESDAY, DECEMBER 12TH, 2012

Digital Test, Fault Tolerance and Reliability

Session Code: C1L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Wednesday, December 12th, 2012
(09:30 - 11:10)

Chairs: Salvador Mir
TIMA, France
Diego Vázquez
Univ. of Seville & IMSE-CNM-CSIC, Spain

09:30 **The Leafs Scan-Chain for Test Application Time and Scan Power Reduction**
M. Chalkia, Y. Tsiatouhas
University of Ioannina, Greece

09:50 **Automatic Selective Hardening Against Soft Errors: a Cost-Based and Regularity-Aware Approach**
S. Pagliarini, A. Ben Dhia, L. Alves de Barros Naviner, J. Naviner
Institut Mines-Telecom, Télécom ParisTech, France

10:10 **Transient Fault Analysis of CORDIC Processor**
T. An, M. Causo, L. Alves de Barros Naviner, P. Matherat
Institut Mines-Telecom, Télécom ParisTech, France

10:30 **A New Fault-Tolerant Architecture for CLBs in SRAM-Based FPGAs**
A. Ben Dhia, L. Alves de Barros Naviner, P. Matherat
Institut Mines-Telecom, Télécom ParisTech, France

10:50 **A Monitoring Infrastructure for FPGA Self-Awareness and Dynamic Adaptation**
C. Gómez Osuna, M. Sánchez Marcos, P. Ituero, M. López-Vallejo
Universidad Politécnica de Madrid, Spain

WEDNESDAY, DECEMBER 12TH, 2012

Multimedia Systems and Signal Processing II

Session Code: C1L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Wednesday, December 12th, 2012
(09:30 - 11:10)

Chair: Sergio Bampi
Universidade Federal do Rio Grande do Sul, Brazil

09:30 **Adaptive Disparity Map Computation for Stereoscopic Video Watermarking**
A. Chammem[1], M. Mitrea[1], F. Prêteux[2]
[1] *Institut Mines - Telecom, France*
[2] *Institut Mines-Telecom, Télécom ParisTech, France*

09:50 **Bayesian Classification and Artificial Neural Network Methods for Lung Cancer Early Diagnosis**
F. Taher, N. Werghi, H. Al-Ahmad
Khalifa University, U.A.E.

10:10 **Embedded Vision System for Early Smoke Detection**
S. Ouerghi, F. Tlili, A. Benazza-Benyahia
Sup'Com / Carthage University, Tunisia

10:30 **Sub-Images Based Image Hashing with Non-Negative Factorization**
S. Prungsinchai, F. Khelifi, A. Bouridane
Northumbria University, UK

10:50 **A Study on the HEVC Performance over Lossy Networks**
B. Oztas, M. Pourazad, P. Nasiopoulos, V. Leung
University of British Columbia, Canada

LECTURE SESSIONS

WEDNESDAY, DECEMBER 12TH, 2012

RF Circuits and Techniques II

Session Code: C2L-A (Lecture)

Location: Room Sevilla I

Date & Time: Wednesday, December 12th, 2012
(11:30 - 13:10)

Chair: Eduard Alarcón
Technical University of Catalunya (UPC), Spain

11:30 **0.4V Low-Power 60-GHz Oscillator in 65nm CMOS**
D. Pepe[1], D. Zito[1,2]
[1] *Tyndall National Institute, Ireland*
[2] *University College Cork, Ireland*

11:50 **Complements on Phase Noise Analysis and Design of CMOS Ring Oscillators**
T. Cronin[1,2], D. Pepe[1], D. Zito[1,2]
[1] *Tyndall National Institute, Ireland*
[2] *University College Cork, Ireland*

12:10 **A Low-Power All-Digital PLL Architecture Based on Phase Prediction**
J. Zhuang[1], R. Staszewski[2]
[1] *Qualcomm, USA*
[2] *Delft University of Technology, Netherlands*

12:30 **A Dead-Zone Free and Linearized Digital PLL**
A. Samarah, A. Chan Carusone
University of Toronto, Canada

12:50 **Feasibility Study Including Detector Non-Idealities of a 95-GHz CMOS SoC Radiometer for Passive Imaging**
L. Mereni[1], D. Pepe[1], D. Zito[1,2]
[1] *Tyndall National Institute, Ireland*
[2] *University College Cork, Ireland*

WEDNESDAY, DECEMBER 12TH, 2012

Emerging Technologies II

Session Code: C2L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Wednesday, December 12th, 2012 (11:30 - 13:10)

Chair: Fernando Corinto
Politecnico di Torino, Italy

11:30 **Non-Volatile Memory Circuits for FIMS and TAS Writing Techniques on Magnetic Tunnelling Junctions**
V. Silva[1], M. Véstias[2], H. Neto[1], J. Fernandes[1]
[1] *INESC-ID / IST / Universidade Técnica de Lisboa, Portugal*
[2] *INESC-ID / ISEL / IPL, Portugal*

11:50 **Validation and Analysis of Negative Differential Resistance of Single-Electron Transistor with Conductance Model**
X. Chen, Z. Xing, B. Sui
National University of Defense Technology, China

12:10 **Low-Noise Dual-Channel Current Amplifier for DNA Sensing with Solid-State Nanopores**
M. Carminati[1], G. Ferrari[1], M. Sampietro[1], A. Ivanov[2], T. Albrecht[2]
[1] *Politecnico di Milano, Italy*
[2] *Imperial College London, UK*

12:30 **CMOS Active Column Sensor for Biodetection Applications Based on Surface Plasmon Resonance**
A. Salazar[1], S. Camacho-León[1], S. Martínez-Chapa[1], O. Rossetto[2]
[1] *Tecnológico de Monterrey, Mexico*
[2] *Laboratoire de Physique Subatomique et de Cosmologie, France*

12:50 **Modeling and Analysis of Through Silicon via: Electromagnetic and Device Simulation Approach**
K. Salah[1], A. Elrouby[1], H. Ragai[2], Y. Ismail[3]
[1] *Mentor Graphics, Egypt*
[2] *Ain-Shams University, Egypt*
[3] *American University in Cairo, Egypt*

LECTURE SESSIONS

WEDNESDAY, DECEMBER 12TH, 2012

Variability-Aware Design and Noise Mitigation

Session Code: C2L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Wednesday, December 12th, 2012
(11:30 - 13:10)

Chair: Magdy Bayoumi
University of Louisiana, USA

11:30 **CEMS-PG: a Parametrized Algorithm for Balanced Partitioning and Wakeup of Power Gated Circuits**
S. Farah, M. Bayoumi
University of Louisiana at Lafayette, USA

11:50 **Static Read Stability and Write Ability Metrics in FinFET Based SRAM Considering Read and Write-Assist Circuits**
H. Jeong, Y. Yang, J. Lee, J. Kim, S. Jung
Yonsei University, South Korea

12:10 **Statistical Leakage Analysis Using the Deterministic Modeling of Cell Leakage Current**
J. Kim, Y. Kim
POSTECH, South Korea

12:30 **Uncertainty in DLL Deskewing Schemes**
M. Figueiredo[1], R. Aguiar[2]
[1] *Polytechnic Institute of Leiria, Portugal*
[2] *Universidade de Aveiro, Portugal*

12:50 **High-Drive Capability Buffer for Highly Variable Resistive Loads**
E. Covi, A. Cabrini, G. Torelli
Università degli Studi di Pavia, Italy

WEDNESDAY, DECEMBER 12TH, 2012

Nonlinear Circuits and Systems II

Session Code: C2L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Wednesday, December 12th, 2012 (11:30 - 13:10)

Chair: Michael Peter Kennedy
University College, Cork, Ireland

11:30 **Should Delta Sigma Modulators Used in AC Motor Drives Be Adapted to the Mechanical Load of the Motor?**
S. Callegari[1], F. Bizzarri[2]
[1] *Università di Bologna, Italy*
[2] *Politecnico di Milano, Italy*

11:50 **Design of a Low Complexity S-Box Based on a Piecewise Linear Chaotic Map**
D. Yoshioka
Sojo University, Japan

12:10 **On Current Control Method for Single-Phase AC Resistance Spot Welding**
K. Zhou, L. Cai
Hong Kong University of Science and Technology, China

12:30 **A Brief Analysis of the Main SPICE Models of the Memristor**
J. Albo-Canals[1], G. Pazienza[2]
[1] *Universitat Ramon Llull, Spain*
[2] *Pazmany University, Hungary*

LECTURE SESSIONS

WEDNESDAY, DECEMBER 12TH, 2012

Power Management Circuits

Session Code: C3L-A (Lecture)

Location: Room Sevilla I

Date & Time: Wednesday, December 12th, 2012
(14:40 - 16:20)

Chair: Eduard Alarcón
Technical University of Catalunya (UPC), Spain

14:40 **Field Programmable Switched Capacitor Voltage Converter**
C. Li, J. Cosp, H. Martinez-García
Universitat Politecnica de Catalunya, Spain

15:00 **A Reconfigurable Buck-Boost Switched Capacitor Converter with Adaptive Gain and Discrete Frequency Scaling Control**
L. George, T. Lehmann, T. Hamilton
University of New South Wales, Australia

15:20 **Design of a Capacitorless Low-Dropout Voltage Regulator with Fast Load Regulation in 130nm CMOS**
A. Souza[1,2], S. Bampi[2]
[1] *CEITEC-SA Semiconductors, Brazil*
[2] *Universidade Federal do Rio Grande do Sul, Brazil*

WEDNESDAY, DECEMBER 12TH, 2012

Neural Networks and Nonlinear Circuits

Session Code: C3L-B (Lecture)

Location: Room Andalucía 8

Date & Time: Wednesday, December 12th, 2012 (14:40 - 16:20)

Chair: Ricardo Carmona
IMSE-CNM-CSIC, Spain

14:40 **Dedicated FPGA Communication Architecture and Design for a Large-Scale Neuromorphic System**
V. Thanasoulis, J. Partzsch, S. Hartmann, C. Mayr, R. Schüffny
Technische Universität Dresden, Germany

15:00 **Towards AER VITE: Building Spike Gate Signal**
F. Perez-Peña[1], A. Morgado-Estevez[1], C. Rioja-Del-Rio[1], A. Linares-Barranco[2], A. Jimenez-Fernandez[2], J. Lopez-Coronado[3], J. Muñoz-Lozano[3]
[1] *Universidad de Cádiz, Spain*
[2] *Universidad de Sevilla, Spain*
[3] *Universidad Politécnica de Cartagena, Spain*

15:20 **Picosecond Pulse Generation with Nonlinear Transmission Lines in 90-nm CMOS for mm-Wave Imaging Applications**
P. Indirayanti, W. Volkaerts, P. Reynaert, W. Dehaene
Katholieke Universiteit Leuven, Belgium

LECTURE SESSIONS

WEDNESDAY, DECEMBER 12TH, 2012

Energy Efficient High-level Design and Modeling Techniques

Session Code: C3L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Wednesday, December 12th, 2012
(14:40 - 16:20)

Chairs: Malgorzata Chrzanowska-Jeske
Portland State University, USA
Antonio Acosta
Univ. of Seville & IMSE-CNM-CSIC, Spain

14:40 **High Level Modeling of Signal Integrity in Field Bus Communication with SystemC-AMS**
R. Wang, J. Denoulet, S. Feruglio, F. Vallette, P. Garda
Université Pierre et Marie Curie, France

15:00 **IMOSIM: Exploration Tool for Instruction Memory Organisations Based on Accurate Cycle-Level Energy Modelling**
A. Artes[1], J. Ayala[1], F. Catthoor[2]
[1] *Complutense University of Madrid, Spain*
[2] *IMEC, Belgium*

15:20 **Power Efficiency of Digit Level Polynomial Basis Finite Field Multipliers in GF(2^283)**
S. Hashemi Namin, H. Wu, M. Ahmadi
University of Windsor, Canada

15:40 **A High-Throughput ECC Architecture**
E. Amini, Z. Jeddi, M. Bayoumi
University of Louisiana at Lafayette, USA

16:00 **Energy-Efficient Multi-Task Computing on MPSoCs: a Case Study from a Memory Perspective**
R. Westphal, J. Güntzel, L. Santos
Universidade Federal de Santa Catarina, Brazil

WEDNESDAY, DECEMBER 12TH, 2012

Communication Algorithms and Building Blocks

Session Code: C3L-D (Lecture)

Location: Room Andalucía 6

Date & Time: Wednesday, December 12th, 2012 (14:40 - 16:20)

Chair: Piedad Brox
IMSE-CNM-CSIC, Spain

14:40 **Second-Order TDTL with Initialization Process**
M. Al-Qutayri[1], S. Al-Araji[1], J. Jeedella[1], O. Al-Ali[2], N. Anani[2]
[1] *Khalifa University, U.A.E.*
[2] *Manchester Metropolitan University, UK*

15:00 **Encoding Sequence Design for a Reduced Complexity Time Synchronization Approach for OFDM Systems**
L. Nasraoui, L. Najjar Atallah, M. Siala
Sup'Com, Tunisia

15:20 **Test Setup for Error Vector Magnitude Measurement on WLAN Transceivers**
V. Fialho, F. Fortes, M. Vieira
Instituto Superior de Engenharia de Lisboa, Portugal

15:40 **A Hybrid Algorithm for Range Estimation in RFID Systems**
K. Thangarajah, R. Rashizadeh, S. Erfani, M. Ahmadi
University of Windsor, Canada

16:00 **Discrete Cosine Transform Type-IV-Based Multicarrier Modulators in Frequency Offset Channels**
P. Amo-López[1], M. Domínguez-Jiménez[2], G. Sansigre[2], D. Sanz de la Fuente[1], F. Cruz-Roldán[1]
[1] *Universidad de Alcalá, Spain*
[2] *Universidad Politécnica de Madrid, Spain*

LECTURE SESSIONS

WEDNESDAY, DECEMBER 12TH, 2012

Sensors and Imagers

Session Code: C4L-A (Lecture)

Location: Room Sevilla I

Date & Time: Wednesday, December 12th, 2012 (16:40 - 18:20)

Chair: Eduard Alarcón
Technical University of Catalunya (UPC), Spain

16:40 **A CMOS Pixel Sensor with 4-bit Column-Parallel Self-Triggered ADC for the ILC Vertex Detector**
L. Zhang, F. Morel, C. Hu-Guo, A. Himmi, A. Dorokhov, Y. Hu
Université de Strasbourg, France

17:00 **A Low Noise High Dynamic Range Analog Front-End ASIC for the AGIPD XFEL Detector**
X. Shi[1], R. Dinapoli[1], D. Greiffenberg[1], B. Henrich[1], A. Mozzanica[1], B. Schmitt[1], H. Krüger[2], H. Graafsma[3], A. Klyuev[3], A. Marras[3], U. Trunk[3]
[1] *Paul Scherrer Institute, Switzerland*
[2] *Universität Bonn, Germany*
[3] *Deutsches Elektronen Synchrotron, Germany*

17:20 **Sense/Drive Architecture for CMOS-MEMS Accelerometers with Relaxation Oscillator and TDC**
P. Michalik[1], J. Madrenas[1], D. Fernández[2]
[1] Universitat Politecnica de Catalunya, Spain
[2] *Baolab Microsystems, Spain*

17:40 **Low Power Time-of-Flight 3D Imager System in Standard CMOS**
P. Kumar, E. Charbon, R. Staszewski, A. Borowski
Delft University of Technology, Netherlands

18:00 **A Double-Delta Compensating Technique for Pulse-Frequency Modulation CMOS Image Sensor**
T. Tsai, R. Hornsey
York University, Canada

WEDNESDAY, DECEMBER 12TH, 2012

Advances in Nanoscale Devices and Circuits: Modeling, Design, Testing

Session Code: C4L-B (Lecture) (Special Session)

Location: Room Andalucía 8

Date & Time: Wednesday, December 12th, 2012
(16:40 - 18:20)

Chairs: Spiros Nikolaidis
Aristotle Univ. of Thessaloniki, Greece
Abdoul Rjoub
Jordan University of Science and Technology, Jordan

16:40 **Design of Adaptive Nano/CMOS Neural Architectures**
T. Serrano-Gotarredona, B. Linares-Barranco
Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain

17:00 **Compact Modeling for the Transcapacitances of Undoped or Lightly Doped Nanoscale Cylindrical Surrounding Gate MOSFETs**
N. Fasarakis[1], A. Tsormpatzoglou[1], D. Tassis[1], K. Papathanasiou[1], C. Dimitriadis[1], G. Ghibaudo[2]
[1] *Aristotle University of Thessaloniki, Greece*
[2] *IMEP, MINATEC, France*

17:20 **Estimating the Starting Point of Conduction in Nanoscale CMOS Gates**
D. Tzagkas[1], S. Nikolaidis[1], A. Rjoub[2]
[1] *Aristotle University of Thessaloniki, Greece*
[2] *Jordan University of Science and Technology, Jordan*

17:40 **Testing Wireless Transceivers' RF Front-Ends Utilizing Defect-Oriented BIST Techniques**
L. Dermetzoglou[1], J. Liaperdos[1], A. Arapoyanni[1], Y. Tsiatouhas[2]
[1] *University of Athens, Greece*
[2] *University of Ioannina, Greece*

18:00 **Fast and Accurate Estimation of Gain and Unity-Gain Bandwidth of an OpAmp**
R. Picos, J. Font-Rossello, E. Garcia-Moreno, A. Teruel
Universitat de les Illes Balears, Spain

LECTURE SESSIONS

WEDNESDAY, DECEMBER 12TH, 2012

Algorithms and Processors

Session Code: C4L-C (Lecture)

Location: Room Andalucía 7

Date & Time: Wednesday, December 12th, 2012
(16:40 - 18:20)

Chair: Javier Castro
University of Seville, Spain

16:40 **FIR Fractional Hilbert Transformers with Raised-Cosine Magnitude Response**
G. Molnar, M. Vucic
University of Zagreb, Croatia

17:00 **Conflict Free, Parallel Memory Access for Radix-2 FFT Processors**
N. Polychronakis, D. Reisis, E. Tsilis, I. Zokas
National and Kapodistrian University of Athens, Greece

17:20 **An Efficient 2-D Jacobian Iteration Modeling for Image Interpolation**
A. Kumar[1], N. Agarwal[1], J. Bhadviya[1], A. Tiwari[2]
[1] *LNM Institute of Information Technology, Jaipur, India*
[2] *Indian Institute of Technology Rajasthan, India*

17:40 **A Switching Based Adaptive Image Interpolation Algorithm**
N. Agarwal[1], A. Kumar[1], J. Bhadviya[1], A. Tiwari[2]
[1] *LNM Institute of Information Technology, Jaipur, India*
[2] *Indian Institute of Technology Rajasthan, India*

18:00 **A Highly Parallelized Processor for Face Detection Based on Haar-Like Features**
H. Qin, L. Tian, Z. Hu
South China University of Technology, China

ICECS holds a PhD Competition where participants can compete with live demos. Six students from four different countries have been accepted in the submission procedure.
The following jury members will adjudicate the ICECS 2012 PhD Competition:
- Fernando Medeiro (*AnaFocus, Spain*)
- Michael Peter Kennedy (*University College Cork, Ireland*)
- Valentino Liberali (*Università degli Studi di Milano, Italy*)
- Malgorzata Chrzanowska-Jeske (*Portland State Univ., USA*)
- Joaquín Ceballos, (*IMSE-CNM-CSIC, Spain*)

The participants in this competition will present their work briefly. After the presentations, all live demonstrators will be exposed simultaneously in room Sevilla I.
The award delivery will take place during the gala dinner and the winners will be each awarded with a tablet.
ICECS 2012 Organization Committee encourages your attendance at this event.

TUESDAY, DECEMBER 11TH, 2012

PhD Competition

Session Code:	B4L-A (Lecture)
Location:	Room Sevilla I
Date & Time:	Tuesday, December 11th, 2012 (17:10 - 19:10)
Chair:	Fernando Medeiro *Anafocus, Spain*

A Telemetry Operated Vestibular Prosthesis
D. Cirmirakis, D. Jiang, A. Demosthenous, N. Donaldson, T. Perkins
University College London, UK

Model-Based Design for Selecting Fingerprint Recognition Algorithms for Embedded Systems
R. Arjona, I. Baturone
Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain

Electrical Characterization of a C-Element with LiChEn
M. Moreira, N. Calazans
Pontifícia Universidade do Rio Grande do Sul, Brazil

Control and Acquisition System for a High Dynamic Range CMOS Image Sensor
S. Vargas-Sierra, G. Liñán-Cembrano, Á. Rodríguez Vázquez
Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain

Long-Term Pulse Stimulation and Recording in an Accelerated Neuromorphic System
V. Thanasoulis, J. Partzsch, B. Vogginger, C. Mayr, R. Schüffny
Technische Universität Dresden, Germany

Real-Time FPGA Connected Component Labeling System
E. Calvo-Gallego[1], A. Cabrera Aldaya[2], P. Brox[1],
S. Sánchez-Solano[1]
[1] *Universidad de Sevilla / Instituto de Microelectrónica de Sevilla, Spain*
[2] *Instituto Superior Politécnico José Antonio Echevarría, Cuba*

The ICECS Poster Exhibition will be held in the Exhibition Area in the basement near "Atrio III" (please refer to the meeting rooms floorplan included in this program). The posters will be introduced by their authors during two different Poster Briefing Sessions on Monday 10th and Tuesday 11th (please refer to the timetables below). Posters will be then displayed in the Poster Area on Tuesday 11th from 17:10 to 19:10.

MONDAY, DECEMBER 10TH, 2012

Poster Briefing Session 1

Session Code: B4P-G (Poster)

Location: Sevilla I

Date & Time: Monday, December 10th, 2012 (**16:40 - 17:10**)

Chair: José M. de la Rosa
Univ. of Seville & IMSE-CNM-CSIC, Spain

A 500 MHz to 6 GHz Frequency Synthesizer Architecture for Cognitive Radio Applications
Z. El Alaoui Ismaili, F. Nabki, W. Ajib, M. Boukadoum
Université du Québec à Montréal, Canada

Understanding Large Swing and Low Swing Operation in DyCML Gates
T. Borges[1], E. Martins[1], L. Alves[1,2]
[1] *Universidade de Aveiro, Portugal*
[2] *Instituto de Telecomunicações, Portugal*

A Fully Complementary and Fully Differential Self-Biased Asynchronous CMOS Comparator
V. Milovanovic, H. Zimmermann
Technische Universität Wien, Austria

Channel Mismatch Background Calibration for Pipelined Time Interleaved ADCs
A. Mrassy[1], M. Dessouky[1,2]
[1] *Ain Shams University, Egypt*
[2] *Mentor Graphics Corp., Egypt*

A Low-Power Single-Slope Analog-to-Digital Converter with Digital PVT Calibration
Y. Osaki, T. Hirose, K. Tsubaki, N. Kuroki, M. Numa
Kobe University, Japan

SkyFlash EC Project: Architecture for a 1Mbit S-Flash for Space Applications
A. Arbat[1], C. Calligaro[1], V. Dayan[2], E. Pikhay[2], Y. Roizin[2]
[1] *RedCat Devices, Italy*
[2] *TowerJazz, Israel*

A Practical Method for Modeling Amplifier Nonlinearities
S. Ali, S. Tanner, P. Farine
École Polytechnique Fédérale de Lausanne, Switzerland

Performances and Trends in Millimeter-Wave CMOS Voltage Controlled Oscillators
M. Voicu[1,2], D. Pepe[1], D. Zito[1,2]
[1] *Tyndall National Institute, Ireland*
[2] *University College Cork, Ireland*

A Multi-Valued 350nm CMOS Voltage Reference
N. Lourenço[1], L. Alves[1,2], J. Cura[1,2]
[1] *Universidade de Aveiro, Portugal*
[2] *Instituto de Telecomunicações, Portugal*

Layout Stress and Proximity Aware Analog Design Methodology
A. Zein[1], A. Tarek[1], M. Bahr[1], M. Dessouky[1,2], H. Eissa[2], A. Ramadan[2], A. Tosson[2]
[1] *Ain Shams University, Egypt*
[2] *Mentor Graphics, Egypt*

A 1.1 V 82.3dB Audio Delta-Sigma ADC Using Asynchronous SAR Type Quantizer
Y. Park[1], T. Kwon[1], K. Cho[1], Y. Kwak[1], G. Ahn[1], C. Shin[2], M. Lee[2], S. You[2], H. Park[2]
[1] *Sogang University, South Korea*
[2] *Samsung Electronics, South Korea*

Design Tradeoffs for Rad-Hard Voltage Controlled Crystal Oscillators
J. Cardoso
Universidade do Porto, Portugal

Design of Three-Stage Nested-Miller Compensated Operational Amplifiers Based on Settling Time
H. Aminzadeh
Payame Noor University, Iran

TUESDAY, DECEMBER 11TH, 2012

Poster Briefing Session 2

Session Code: B4P-H (Poster)

Location: Sevilla I

Date & Time: Tuesday, December 11th, 2012 (**16:40 - 17:10**)

Chair: José M. de la Rosa
Univ. of Seville & IMSE-CNM-CSIC, Spain

A Mixed-Signal Front-End ASIC for EEG Acquisition System
H. Zhou, M. Voelker, J. Hauer
Fraunhofer-Institut für Integrierte Schaltungen, Germany

LC Tank Full Bridge Control for Large Coil Variations
J. Merino Panades, C. Dehollain
École Polytechnique Fédérale de Lausanne, Switzerland

Efficient Area and Power Multiplication Part of FFT Based on Twiddle Factor Decomposition
S. Ghissoni[1], E. Costa[2], J. Monteiro[3], R. Reis[4]
[1] *Universidade Federal do Pampa, Brazil*
[2] *Universidade Católica de Pelotas, Brazil*
[3] *INESC-ID / IST / Universidade Técnica de Lisboa, Portugal*
[4] *Universidade Federal do Rio Grande do Sul, Brazil*

Offset Measurement Method for Accurate Characterization of BTI-Induced Degradation in Opamps
S. Mahato, P. De Wit, E. Maricau, G. Gielen
Katholieke Universiteit Leuven, Belgium

A Study on MOSFET Rectifiers with Transistors Operating in the Weak Inversion Region
H. Gonçalves[1], M. Martins[1], J. Fernandes[2]
[1] *INESC-ID, Portugal*
[2] *INESC-ID / IST / Universidade Técnica de Lisboa, Portugal*

Return-to-One Dims Logic on 4-Phase M-of-N Asynchronous Circuits
M. Moreira, R. Guazzelli, N. Calazans
Pontifícia Universidade do Rio Grande do Sul, Brazil

An Ultra-Low Power Current Reused CMOS Low Noise Amplifier for X-Band Space Application
S. Yasami, M. Bayoumi
University of Louisiana at Lafayette, USA

Utilization of Multi-Bit Flip-Flops for Clock Power Reduction
Z. Chen, J. Yan
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Critical Path Minimized Raster Scan Hardware Architecture for Computation of the Generalized Hough Transform
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Flip-Flop Design Using Novel Pulse Generation Technique
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Dedicated Hardware Implementation of a Linear Congruence Solver in FPGA
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Analog Fault Diagnosis and Testing by Inverse Problem Technique
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A Non-Coherent BPSK Receiver with Dual Band Filtering for Implantable Biomedical Devices
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A New XOR-Based Content Addressable Memory Architecture
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A Low-Complexity Soft-Decision Decoding Architecture for the Binary Extended Golay Code
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Fullwave-Mode Analysis of Shielded Microstrip Discontinuities on Anisotropic Substrates
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